Design and Simulation of CMOS Ternary Latches Using esim

https://esim.fossee.in/circuit-simulation-project

Name of the participant : Chandru E

Project Guide : Prof. Kishore Venkat

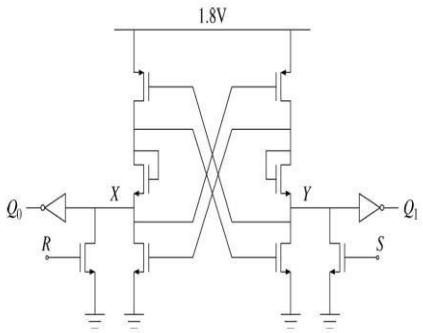
Institute : Chennai Institute Of Technology, at Chennai

University : Anna University

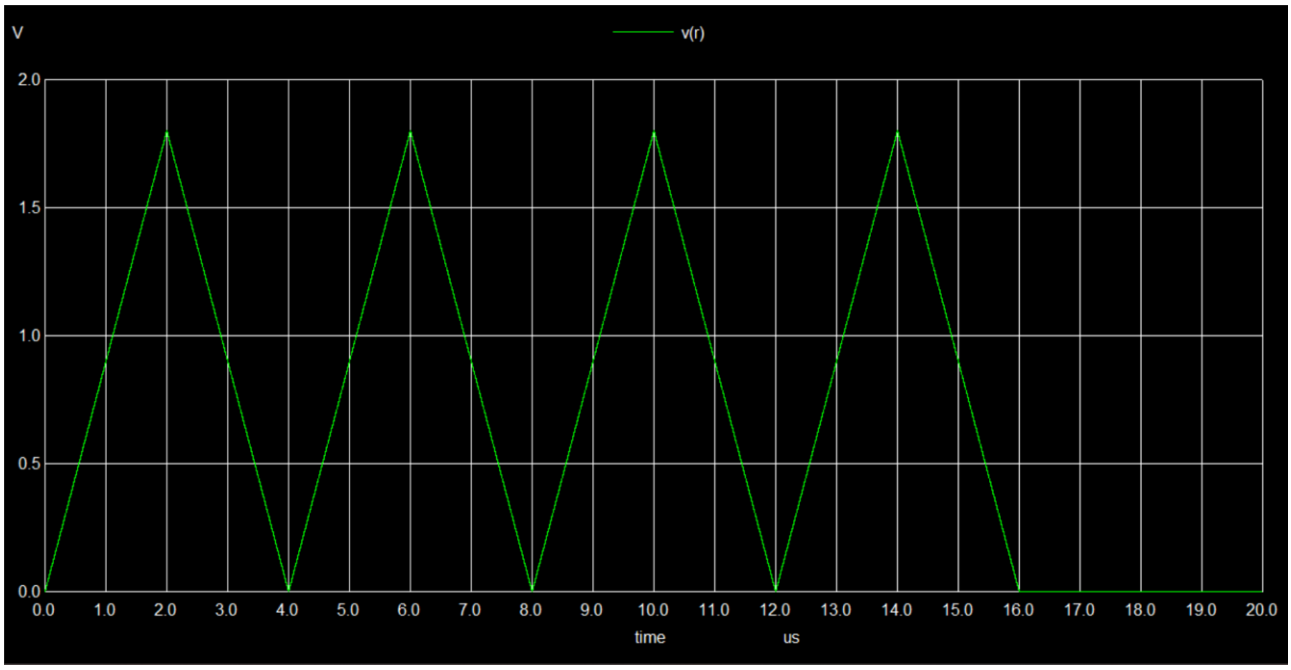
Title of the circuit : Design & Simulation of CMOS Ternary Latches Using esim

Problem Statement : Develop an accurate simulation model for CMOS Ternary Latches to enhance student learning by providing a virtual environment that closely mirrors real-world experimental outcomes **Theory/Description :**

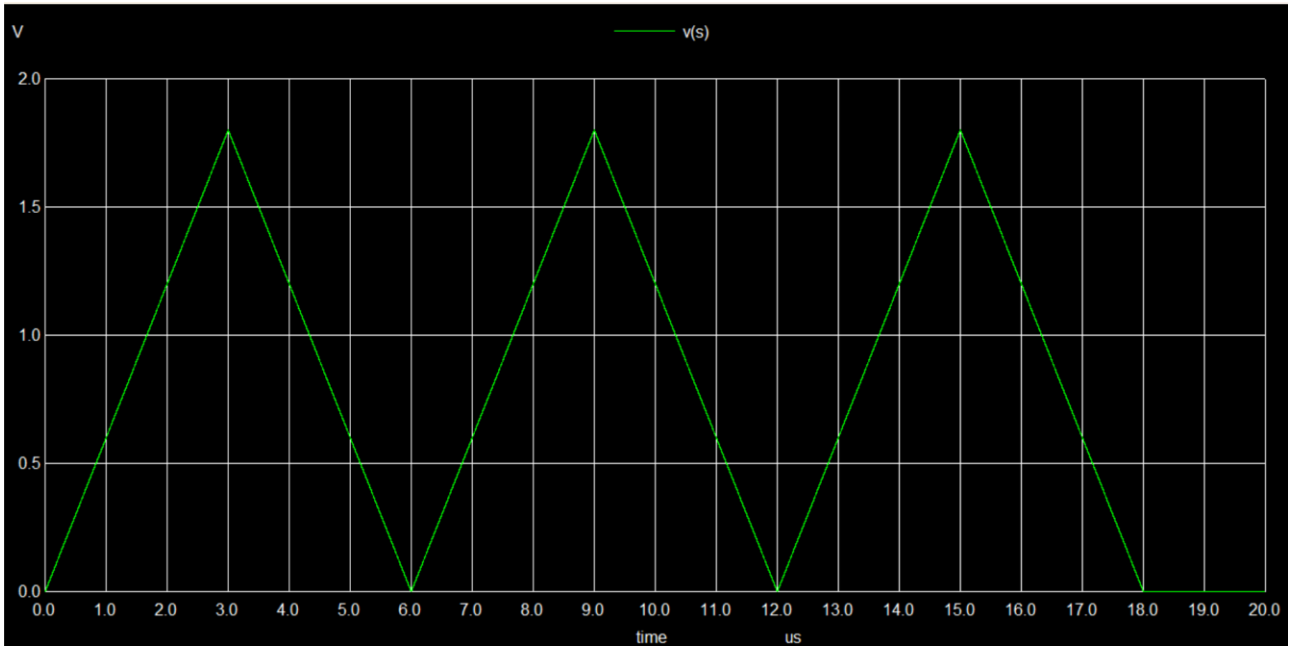
This study describes the design methodology of latches with three stable operating points. Open-loop analysis is used to obtain insight into how a conventional binary latch structure can be modified to yield a ternary latch. Four novel ternary latch structures, compatible with a standard CMOS process, are presented. Properties of each latch, including robustness of the ternary behavior, speed, and power dissipation, are described. Measurement results of four RS ternary flip-flops based on the proposed latch structures, fabricated in a standard 0.18- m CMOS process, are presented. Maximum operating frequency and skew tolerance are reported for each of the four latches **Circuit Diagram(s):**



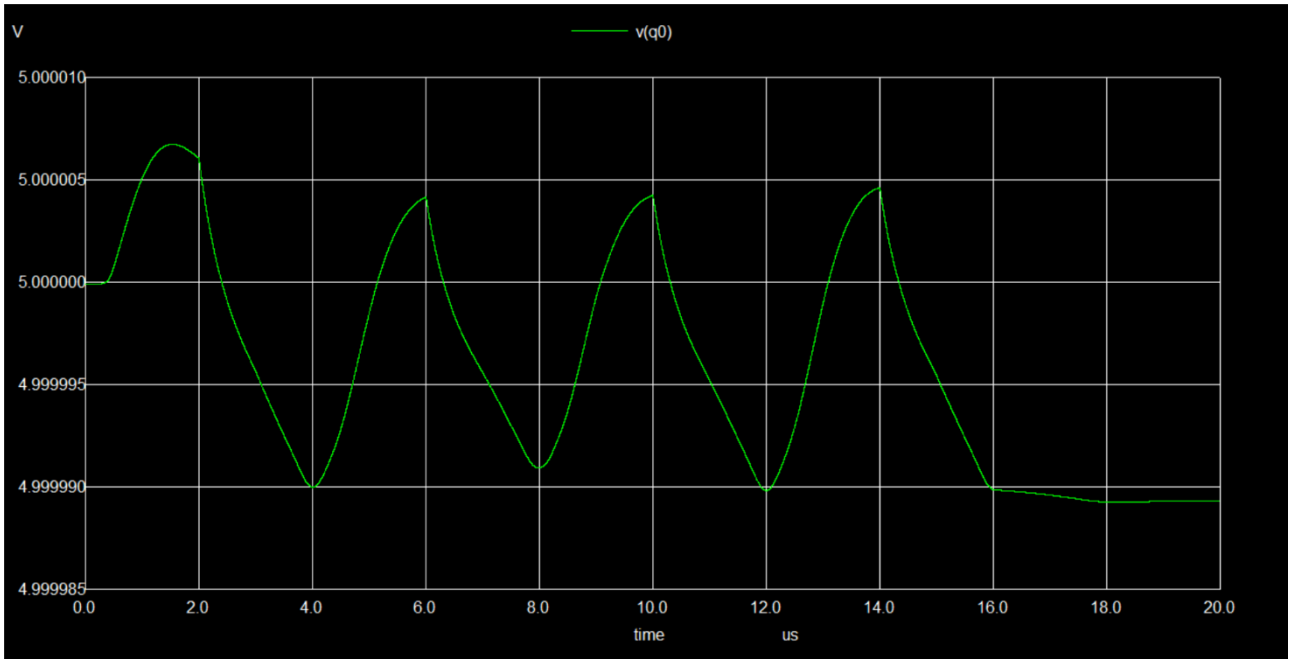
Input waveform for R:



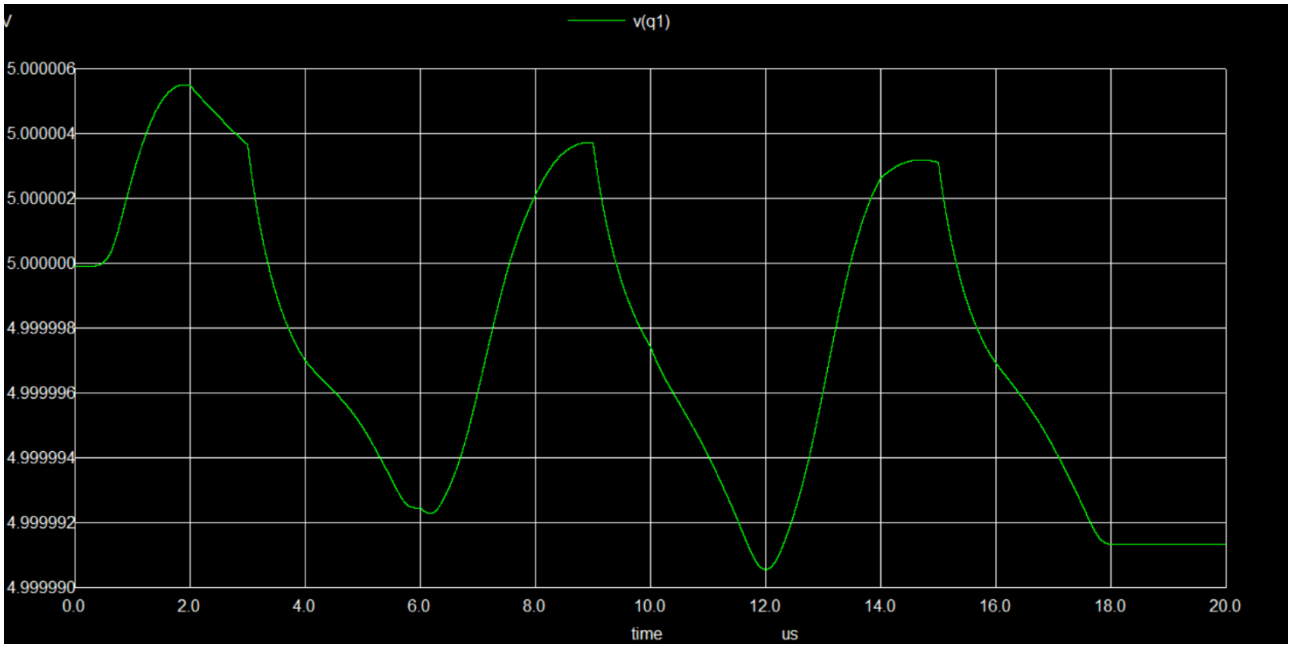
Input Waveform for S:



Output Waveform for Q0:



Output Waveform for Q1:



Source/Reference(s) :

- **Title of the paper :** Design & Simulation of CMOS Ternary Latches
- **Name of the journal/publication :** International Journal of Computer & Mathematical Sciences
- **Author(s) : Shou, X Q Kalantari, N Green, Michael M**
- **Chapter volume pages :** IEEE TRANSACTIONS ONCIRCUITSANDSYSTEMS—I: REGULAR PAPERS , VOL.53,NO.12, DECEMBER2006
- **Link:** **https://www.researchgate.net/publication/3451379_Design_of_CMOS_ternary_latches**