

Research Migration Project

<https://esim.fossee.in/research-migration-project>



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Title of the circuit : Design and Simulation of a Non-Overlapping Two-Phase Clock Generator for Switched-Capacitor Circuits using eSim

Theory/Description :

Switched-capacitor (SC) circuits, charge pumps and pipelined data converters require two complementary clock phases, ϕ_1 and ϕ_2 , that are never logic HIGH at the same instant. If both phases overlap even briefly, charge sharing and short-circuit current paths are created between adjacent SC branches, degrading accuracy and wasting power. A Non-Overlapping Clock (NOC) generator solves this by taking a single input clock and producing ϕ_1 and ϕ_2 with a controlled dead-time gap between them. The circuit is built from two cross-coupled NOR gates (forming a latch that guarantees mutual exclusivity of the two outputs) driven through inverter-based delay chains that set the width of the non-overlap interval, followed by output buffer inverters that sharpen the edges and drive the SC switches.

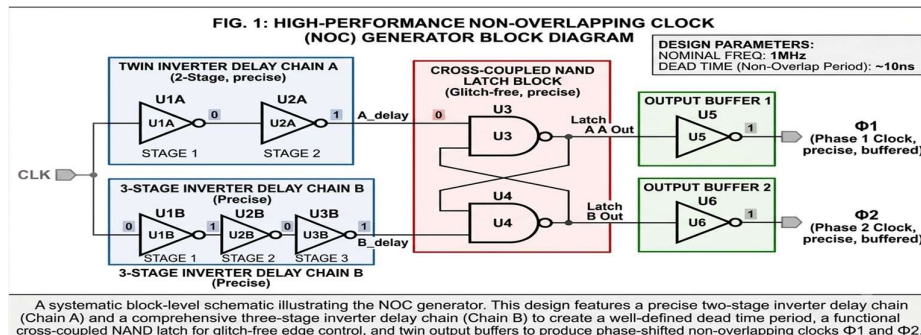
Reason to reproduce with eSim :

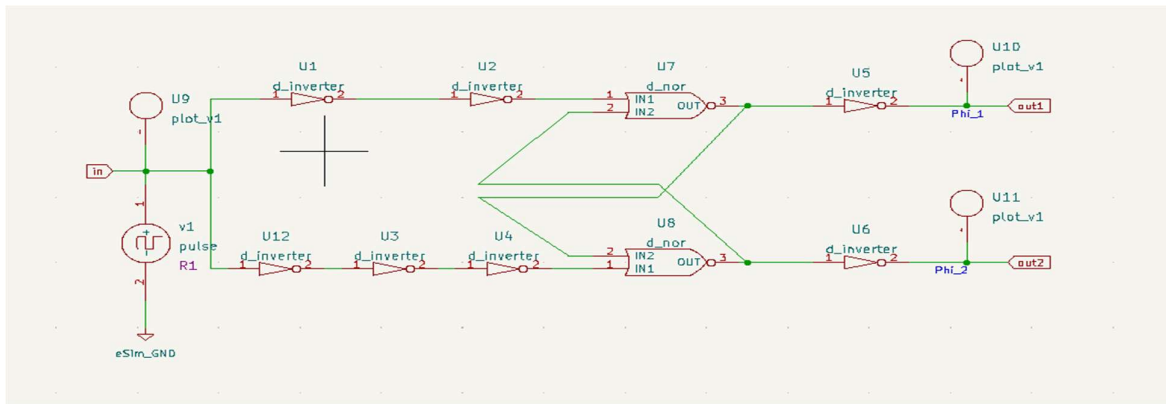
The NOC generator is a single, self-contained digital circuit built entirely from standard logic gates (NOR gates and inverters), making it well suited to a screening-level reproduction in eSim rather than a full commercial IC. Reproducing it validates the paper's claim of a guaranteed, measurable dead-time between ϕ_1 and ϕ_2 and demonstrates eSim's capability to capture sub-gate-delay timing behaviour that is central to mixed-signal and SC circuit design.

Expected Outcome/outputs :

When simulated with a single square-wave input clock, the circuit is expected to produce two complementary output waveforms, ϕ_1 and ϕ_2 , each at the same frequency as the input clock but with a finite, non-zero dead-time gap (set by the inverter delay chain) between the falling edge of one phase and the rising edge of the other. Performance is validated by confirming that ϕ_1 and ϕ_2 are never HIGH simultaneously, and by measuring the dead-time interval as the inverter delay-chain length is varied.

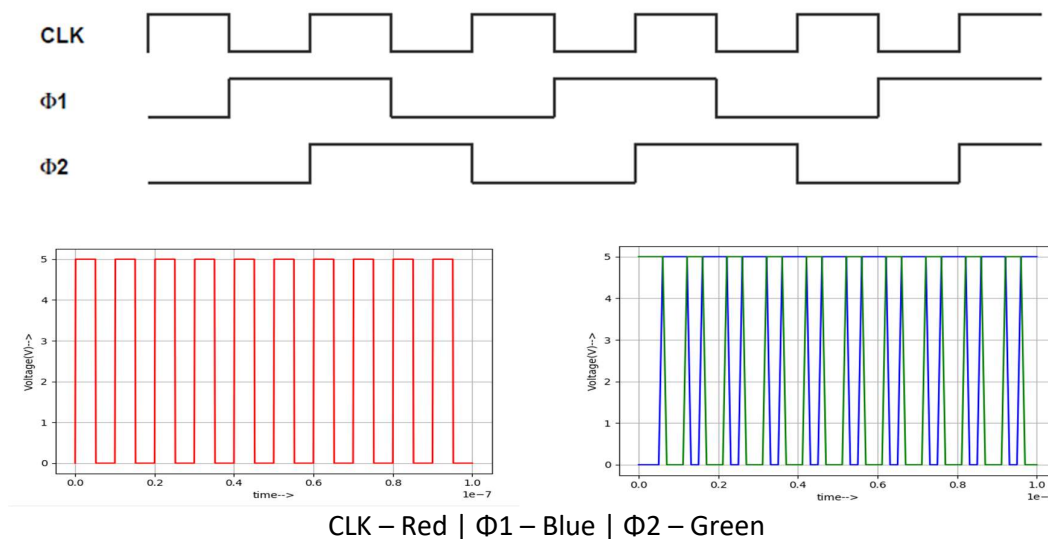
Circuit Diagram :





Expected Results (Input, Output waveforms and/or Multimeter readings) :

Input: a continuous square-wave clock (0V/5V). Outputs: two transient voltage waveforms F1 and F2 of the same period as the input clock, each with reduced duty cycle and a clearly visible dead-time gap between them, as illustrated below.



Research Paper/Journal/etc. :

Title : Non Overlapping Clock (NOC) Generator for Low Frequency Switched Capacitor Circuits

Author : Ashis Kumar Mal, Rishi Todani

Published in : IEEE Students' Technology Symposium (TechSym) 2011, pp. 226–231, DOI:

10.1109/TECHSYM.2011.5783850

Link : <https://ieeexplore.ieee.org/document/5783850/>

Source/Reference(s) :

P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, 2nd Edition — standard reference for non-overlapping clock generation in switched-capacitor circuit design.