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Title of the circuit:

Performance Analysis of 74LS150 Based Multiplexer for Digital Data Selection

Theory/Description:

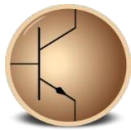
The **74LS150** is a **monolithic 16-to-1 data selector/multiplexer** designed for high-speed digital data selection applications. It integrates multiple transistor-transistor logic (TTL) stages on a single integrated circuit to select one of sixteen input data lines and route the selected signal to a single output. The device uses four binary select inputs (**A, B, C, and D**) to determine which of the sixteen data inputs (**I0-I15**) is transferred to the output. Its active-low output configuration makes it suitable for digital logic implementation, data routing, code conversion, and combinational logic applications.

The internal architecture of the **74LS150** consists of multiple logic stages including input gating, selection circuitry, and an output inverter. The four select inputs are decoded through internal TTL logic to activate the corresponding data path. Each data input is combined with the appropriate decoded select signals, allowing only the selected input to influence the output. The internal gating network provides high-speed switching and reliable logic-level operation. Since the output is active-low, the selected input appears in inverted form at the output, which can also be useful when implementing Boolean functions directly using the multiplexer.

The output section of the **74LS150** provides a TTL-compatible signal that can be connected to subsequent digital logic circuits. The device operates from a standard **5 V supply** and is designed to provide relatively high switching speed with low power consumption compared with earlier standard TTL implementations. The **74LS150** can be used in applications such as **digital data selection, signal routing, Boolean function generation, parallel-to-serial data selection, code conversion, and digital control systems**. Its 16-input architecture reduces the number of separate logic gates required for complex data-selection operations, making it a practical building block for digital systems.

Reason to reproduce with eSim:

The **74LS150** is a **16-to-1 multiplexer (data selector)** widely used in digital systems for selecting one of sixteen input signals and transferring it to a single output. Recreating the **74LS150** in **eSim** expands the FOSSEE open-source digital IC library with an accurate simulation model for research, education, and digital circuit design.



Recreating the complete **gate/transistor-level internal architecture** rather than using a simple functional block model allows users to study the actual operation of the input selection, decoding, logic gating, and output stages. Verification of the recreated model against the original **74LS150 datasheet** ensures that its logic functionality, propagation behavior, and electrical characteristics are represented reliably. Once validated, this model can serve as a foundation for studying **multiplexing, digital data routing, Boolean function implementation, logic design, and educational experiments** using open-source EDA tools.

Expected Outcome/outputs:

A fully functional **transistor-level 74LS150 16-to-1 multiplexer model** in eSim that accurately reproduces the logical behavior and operating characteristics specified in the datasheet.

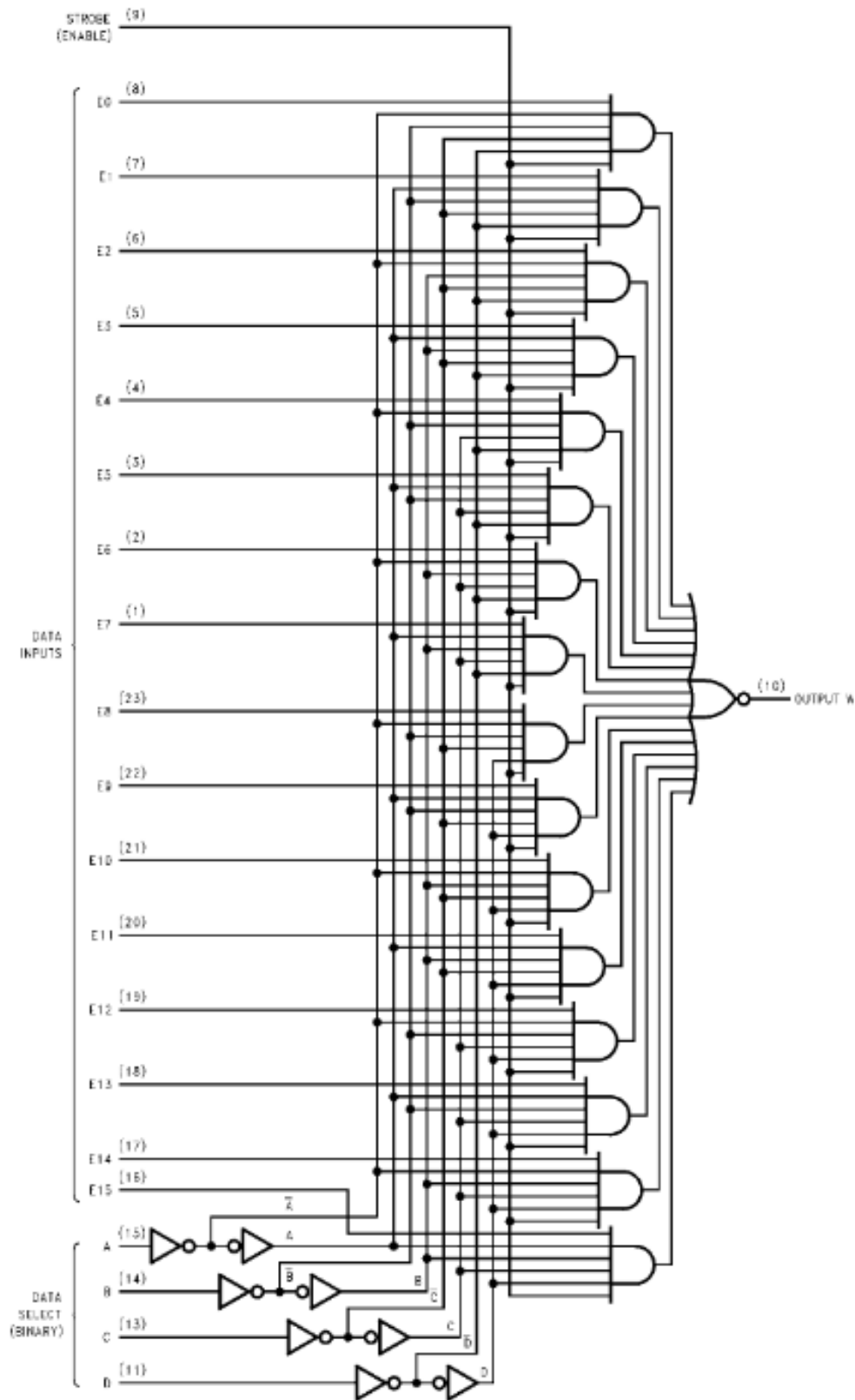
Validation performed by applying different combinations of **16 data inputs and 4 select inputs** to verify correct data selection, output inversion, switching operation, and functional accuracy

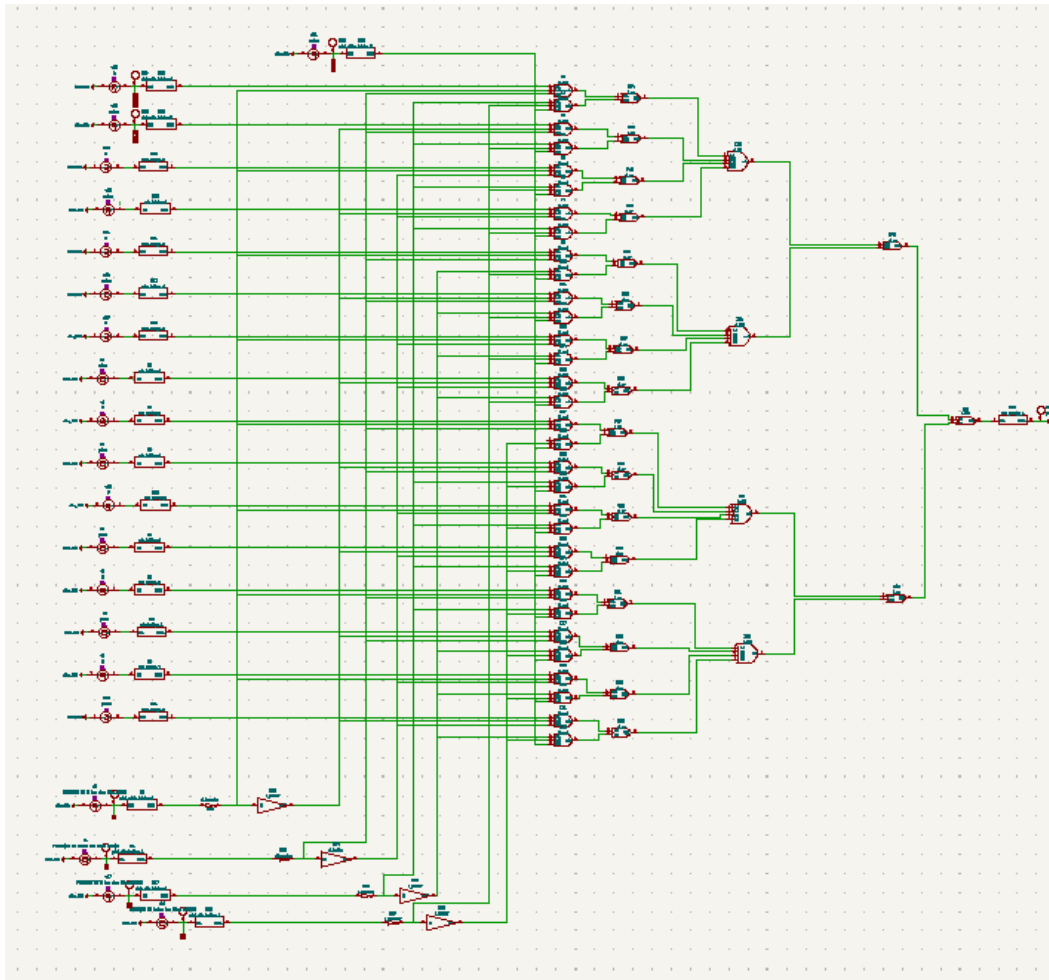
Successful verification indicating that the **74LS150 eSim model** is suitable for deployment in other digital applications requiring **data selection, signal routing, Boolean function implementation, and multiplexing operations**.

Research Migration Project

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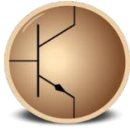
Circuit Diagram(s):



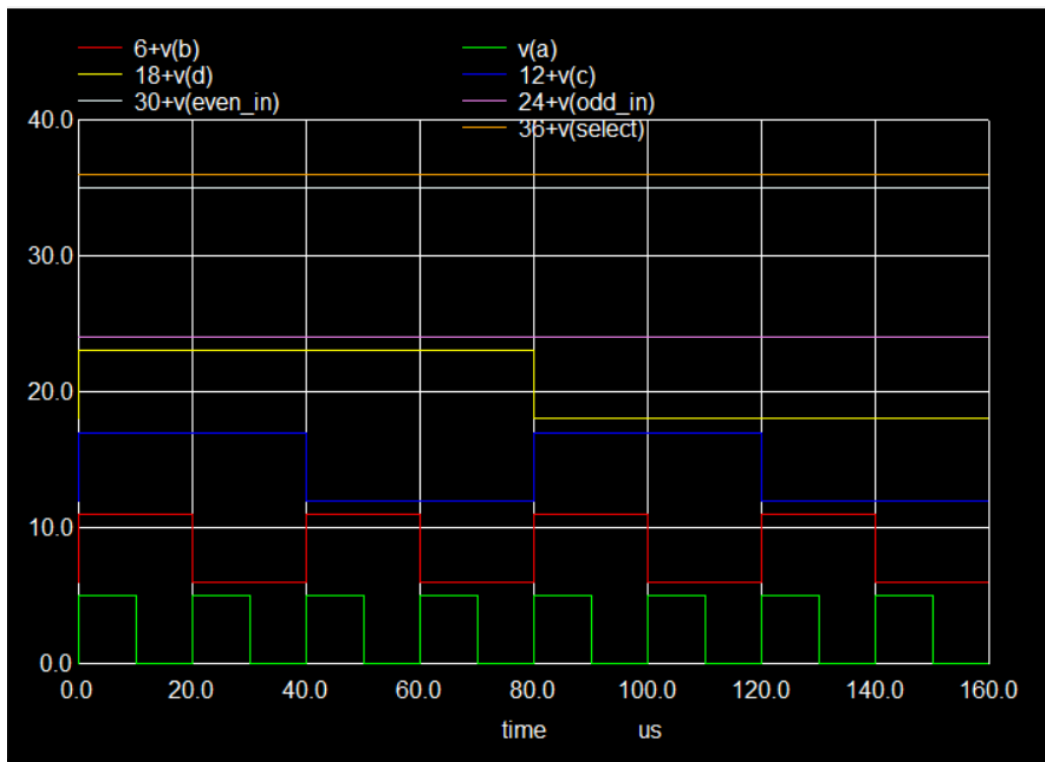


Circuit Architecture Breakdown

- **Data Inputs (Far Left):** You have a column of 16 independent input channels. The symbol pairs consist of SPICE voltage sources connected to ADC bridges. These bridges convert analog SPICE voltages into digital logic states (0 or 1) that the XSpice engine can process.
- **Control/Address Lines (Bottom Left):** These represent your a, b, c, and d counter signals. They feed into a series of buffers and inverters to generate a vertical control bus containing both the true and inverted states of each signal.
- **Decoding Matrix (Center Column):** This massive stack of AND gates acts as the address decoder. Each AND gate is wired to a unique combination of the bottom control lines, ensuring that only one of the 16 input paths is active at any given moment.
- **Aggregation Tree (Right Side):** The cascading layers of OR gates funnel the 16 distinct paths down into a single output stream.
- **Final Output (Far Right):** The digital result passes through a DAC bridge, converting the internal logic state back into the analog voltage trace v(out) that you plotted in your transient simulation.



Input Waveform:



The 4-Bit Counter Inputs

- $v(a)$ (Green): Least Significant Bit (LSB). Toggles the fastest with a 20µs period.
- $v(b)$ (Red): Offset by +6. Toggles with a 40µs period.
- $v(c)$ (Blue): Offset by +12. Toggles with an 80µs period.
- $v(d)$ (Yellow): Most Significant Bit (MSB). Offset by +18. Toggles with a 160µs period.
- Result: These four sources step through all 16 possible binary combinations over the simulation.

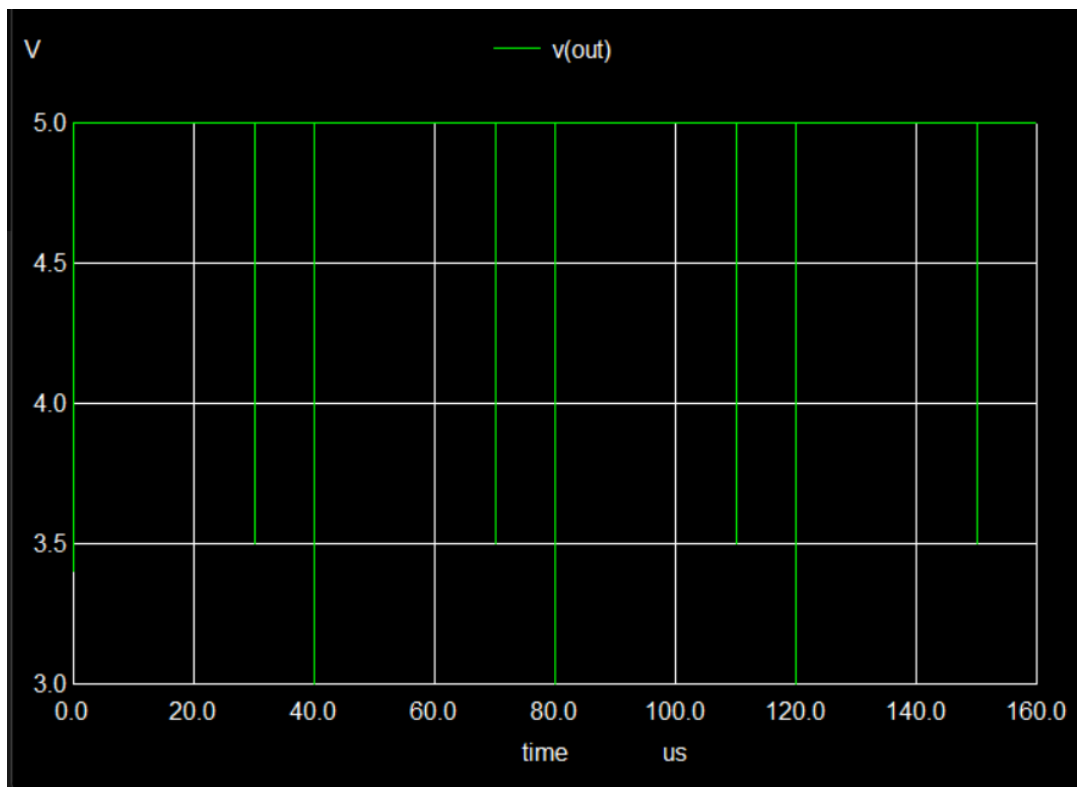
The Static Control Pins

- $v(\text{odd_in})$ (Purple): Offset by +24. Rests exactly at 24, meaning it is tied to 0V (LOW).
- $v(\text{even_in})$ (White): Offset by +30. Rests at 35, meaning it is tied to 5V (HIGH).
- $v(\text{select})$ (Orange): Offset by +36. Rests exactly at 36, meaning it is tied to 0V (LOW).

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Output Waveform:



Output Signal Behavior v(out)

- **Dominant State:** The signal sits almost entirely at 5.0V (Logic HIGH). This means that for the static inputs you provided (select=0, even_in=1, odd_in=0), your combinational logic evaluates to a 1 across all 16 binary states of your counter.
- **Logic Hazards (Glitches):** The sharp, narrow downward spikes you see (at 30 μ s, 40 μ s, 70 μ s, 80 μ s, etc.) are classic digital logic glitches.
- **Cause of Glitches:** These occur at the exact moments your input counter transitions. Because your SPICE netlist defines 1ns propagation delays for the logic gates, unequal delay paths through your 3-input AND/OR gates cause the output to temporarily dip before the correct logic state propagates through.
- **Incomplete Voltage Swings:** Notice that some spikes only drop to ~3.5V rather than a full 0V. The transient logic state is so fast (just a few nanoseconds) that the output node does not have enough time to fully discharge before the circuit resolves itself and drives the pin back to 5V.

In short, your circuit's steady-state output evaluates to HIGH for this specific test case, but the logic is not hazard-free during input transitions.

Research Migration Project

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Research Paper/Journal/etc.:

- S. Brown and Z. Vranesic, *Fundamentals of Digital Logic with VHDL Design*, McGraw-Hill Education.

Relevant for: Multiplexer design, Boolean logic, digital circuit implementation.

- M. M. Mano and M. D. Ciletti, *Digital Design*, Pearson.

Relevant for: Multiplexers, combinational circuits, logic implementation and digital IC design.

- R. J. Tocci, N. S. Widmer, and G. L. Moss, *Digital Systems: Principles and Applications*, Pearson.

Relevant for: Multiplexer operation, TTL logic and digital system applications.

Source/Reference(s):

- Texas Instruments, “SN74LS150 16-Line to 1-Line Data Selector/Multiplexer,” Datasheet.
- Fairchild Semiconductor, “DM74LS150 16-Line to 1-Line Data Selector/Multiplexer,” Datasheet.
- ON Semiconductor, “74LS150 16-to-1 Line Data Selector/Multiplexer,” Datasheet.
- M. M. Mano and M. D. Ciletti, *Digital Design*, Pearson Education.
- R. J. Tocci, N. S. Widmer, and G. L. Moss, *Digital Systems: Principles and Applications*, Pearson.