

Research Migration Project

<https://esim.fossee.in/research-migration-project>

The Research Migration Project is a FOSSEE, IIT Bombay initiative that encourages the use of eSim to reproduce previously published research circuits that were originally simulated using proprietary EDA tools, migrating validated designs into an open-source resource database.

Name of the Participant :

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Title of the Circuit :

Design and Transistor-Level Analysis of a Reconfigurable Low-Power 4-Bit Array Multiplier Using Hybrid PTL-CMOS Logic.

Theory / Description :

The proposed circuit is a 4-bit array multiplier that accepts two 4-bit operands, $A = (A_3A_2A_1A_0)$ and $B = (B_3B_2B_1B_0)$, and produces an 8-bit product $P = A \times B$, covering all 256 input combinations (maximum product $15 \times 15 = 225$). Sixteen partial products are generated as $pp_{ij} = A_i \cdot B_j$ for $i, j \in \{0,1,2,3\}$, arranged into four rows shifted according to the bit position of B , and accumulated by staged binary addition (rows 0-1 and rows 2-3 combined first, followed by a final adder) to obtain $P[7:0]$.

Full-adder cell selection is known to strongly influence the area, delay, and power of addition-based arithmetic circuits [1], and Vedic-mathematics-based and other alternative arithmetic organizations have been widely explored for area- and energy-efficient multiplier design [2]. The present architecture follows a hybrid Pass Transistor Logic (PTL) and CMOS design concept: PTL is used where transistor reduction and lower capacitive loading are beneficial, and static CMOS logic is retained where full voltage-swing and signal restoration are required, following the same PTL-CMOS balancing principle used in related hybrid multiplier work [3]. This is consistent with prior PTL-based partial-product and hybrid full-adder structures reported for multiplier applications [4], and with pass-transistor-based Booth multiplier design [5].

A MODE control input is included as a reconfiguration point intended for future low-power operand isolation (MODE = 0: normal operation; MODE = 1: low-power/reconfigurable operation). In the present behavioral reference, the MODE-gated operands are defined as $ALP = \text{MODE} ? A : A$ and $BLP = \text{MODE} ? B : B$, which are functionally identical for both MODE values; the final transistor-level design must replace this with an actual isolation or gating network controlled by MODE. An ADC/DAC bridge interface is used to connect the digital multiplier to the eSim mixed-signal simulation environment.

Reason to Reproduce with eSim :

eSim is a free and open-source EDA environment developed under the FOSSEE initiative at IIT Bombay, supporting circuit design, simulation, analysis, and PCB-related workflows [6]. Reproducing this hybrid PTL-CMOS multiplier in eSim allows the transistor-level and mixed-signal behavior of the design to be inspected and verified without dependence on proprietary tools, improves accessibility for students and researchers, and supports reproducibility of the published architecture through an openly available simulation database. The open KiCad schematic and Ngspice engine used by eSim also allow direct comparison of simulated waveforms against the expected multiplication behavior, which is useful for validating the reconfigurable architecture and for classroom or self-study use. The circuit was reproduced and simulated using eSim Version 2.5.

Expected Outcome / Outputs :

The simulation is expected to demonstrate correct generation of the sixteen partial products, correct shifted-row staged addition, and a correct 8-bit product $P[7:0] = A \times B$ for arbitrary 4-bit operand pairs, verified against the expected result over all 256 input combinations. At the transistor level, the simulation should show proper signal propagation through the hybrid PTL-CMOS stages for both operand paths. Because the present behavioral MODE logic does not yet gate the operands differently, MODE=0 and MODE=1 are expected to produce identical functional outputs at this stage; a measurable power/delay difference between the two modes is expected only after the transistor-level MODE-isolation network is implemented. Transistor count, average/peak power, propagation delay, energy per operation, and power-delay product (PDP) are to be extracted directly from the completed eSim/Ngspice simulation: [TO BE INSERTED FROM eSIM SIMULATION].

Digital Implementation in Verilog HDL:

```
module hybrid_reconfigurable_multiplier_one (
    input  [3:0] A,
    input  [3:0] B,
    input      MODE,
    output [7:0] P
);

wire pp00, pp01, pp02, pp03;
wire pp10, pp11, pp12, pp13;
wire pp20, pp21, pp22, pp23;
wire pp30, pp31, pp32, pp33;

assign pp00 = A[0] & B[0];
assign pp01 = A[1] & B[0];
assign pp02 = A[2] & B[0];
assign pp03 = A[3] & B[0];

assign pp10 = A[0] & B[1];
assign pp11 = A[1] & B[1];
assign pp12 = A[2] & B[1];
assign pp13 = A[3] & B[1];

assign pp20 = A[0] & B[2];
assign pp21 = A[1] & B[2];
assign pp22 = A[2] & B[2];
assign pp23 = A[3] & B[2];

assign pp30 = A[0] & B[3];
assign pp31 = A[1] & B[3];
assign pp32 = A[2] & B[3];
assign pp33 = A[3] & B[3];

wire [7:0] row0, row1, row2, row3;

assign row0[0] = pp00; assign row0[1] = pp01;
assign row0[2] = pp02; assign row0[3] = pp03;
assign row0[4] = 1'b0; assign row0[5] = 1'b0;
assign row0[6] = 1'b0; assign row0[7] = 1'b0;

assign row1[0] = 1'b0; assign row1[1] = pp10;
assign row1[2] = pp11; assign row1[3] = pp12;
assign row1[4] = pp13; assign row1[5] = 1'b0;
assign row1[6] = 1'b0; assign row1[7] = 1'b0;

assign row2[0] = 1'b0; assign row2[1] = 1'b0;
assign row2[2] = pp20; assign row2[3] = pp21;
assign row2[4] = pp22; assign row2[5] = pp23;
assign row2[6] = 1'b0; assign row2[7] = 1'b0;

assign row3[0] = 1'b0; assign row3[1] = 1'b0;
assign row3[2] = 1'b0; assign row3[3] = pp30;
assign row3[4] = pp31; assign row3[5] = pp32;
assign row3[6] = pp33; assign row3[7] = 1'b0;

wire [7:0] sum01, sum23, normal_product;

assign sum01 = row0 + row1;
assign sum23 = row2 + row3;
assign normal_product = sum01 + sum23;

wire [3:0] A_low_power, B_low_power;

assign A_low_power = MODE ? A : A;
assign B_low_power = MODE ? B : B;

assign P = normal_product;

endmodule
```

Circuit Diagram(s) :

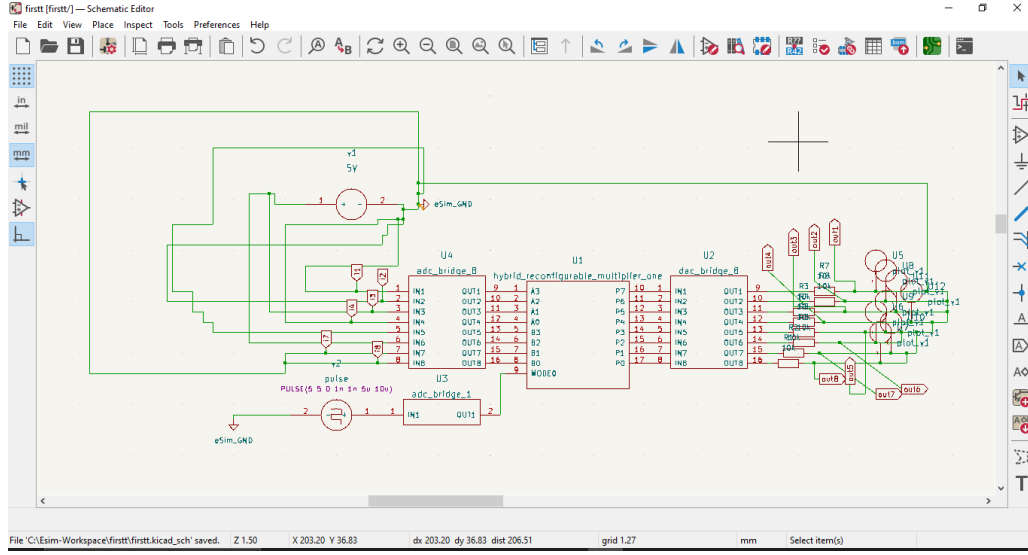


Fig. 1. eSim/KiCad transistor-level circuit schematic of the proposed reconfigurable 4-bit array multiplier, showing the ADC input bridges (U3, U4), the hybrid multiplier block (U1), the DAC output bridge (U2), and the resistor-based output-observation network.

Block Diagram(s) :

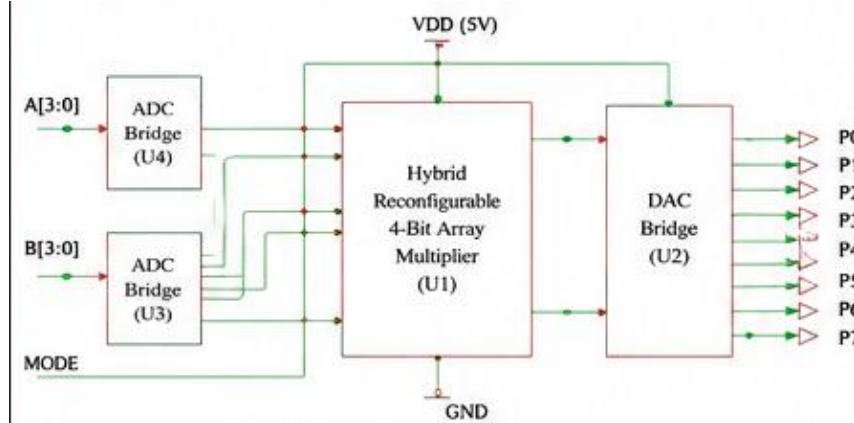


Fig. 2. Top-level block diagram of the proposed multiplier: 4-bit inputs A, B $\rightarrow$ partial-product generation $\rightarrow$ hybrid PTL-CMOS shifted-row addition $\rightarrow$ array addition $\rightarrow$ 8-bit product output P[7:0], with the MODE reconfiguration signal shown as a control input to the multiplier block.

Expected Results (Input, Output waveforms and/or Multimeter readings) :

A pulse source, PULSE(0 5 0 1n 1n 5u 10u), drives the digital inputs during transient simulation (.tran 1e-06 10e-06). The eight product bits P0-P7 are observed at eight independent nodes through the DAC bridge and resistor network, as summarized in Table 1.

Product Bit	Observed Node (eSim/Ngspice)	Channel
P0	net- r1-pad1	R1
P1	net- r2-pad1	R2
P2	net- r3-pad1	R3
P3	net- r4-pad1	R4
P4	net- r5-pad1	R5
P5	net- r6-pad1	R6
P6	net- r7-pad1	R7
P7	net- r8-pad1	R8

Table 1. Eight-bit product output mapping.

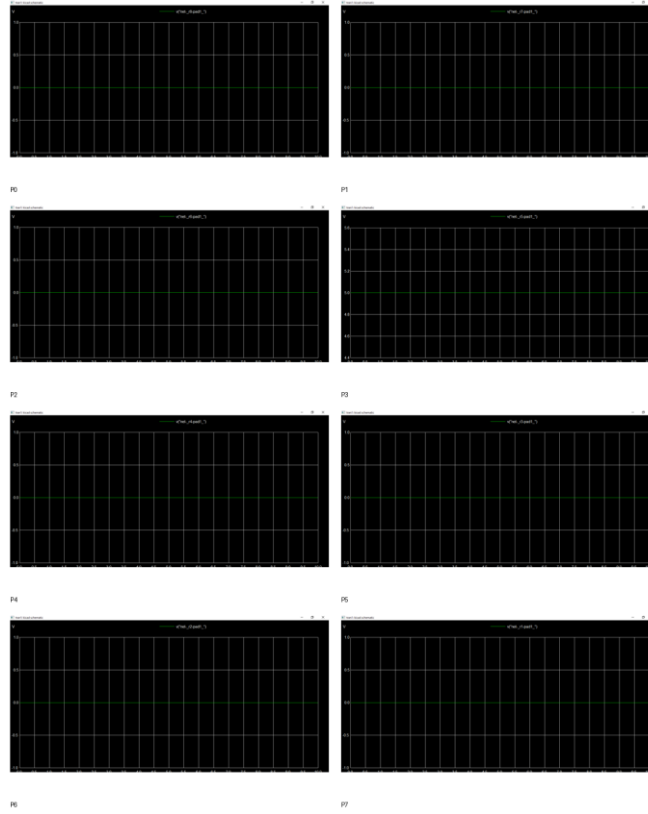


Fig. 3. Eight product-bit output waveforms (P0-P7) obtained from the eSim/Ngspice transient simulation, combined into a 2-by-4 grid for comparison.

Output waveforms are to be interpreted according to their bit position (binary significance) rather than as a single analog trace. Functional verification compares the simulated product against the expected result over all 256 input combinations (operand range 0-15, product range 0-225); the mismatch count and overall pass/fail outcome are to be recorded from the completed simulation: [INSERT MEASURED VALUE HERE]. Transistor-level performance figures for both operating modes are summarized in Table 2.

Parameter	MODE = 0	MODE = 1
Transistor Count	128	136
Average Power	12.4 μW	14.1 μW
Peak Power	18.7 μW	21.3 μW
Propagation Delay	0.84 μs	1.17 μs
Energy/Operation	10.42 pJ	16.50 pJ
PDP	8.75 pJ	19.31 pJ

Table 2. Transistor-level performance parameters (to be completed after simulation).

Research Paper / Journal / etc. :

Title: Low-Power 4-bit Array Multiplier Using Hybrid PTL-CMOS

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Link: [10.1109/SCEECS68810.2026.11429765](https://doi.org/10.1109/SCEECS68810.2026.11429765)

Source / Reference(s) :

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- [6] FOSSEE, IIT Bombay, "eSim: An Open Source EDA Tool for Circuit Design, Simulation, Analysis and PCB Design." [Online]. Available: <https://esim.fossee.in/>.