

Name of the participant :

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Title of the circuit :

eSim-Based Design and Analysis of a Low-Power CMOS Folded Electro -Cascode Amplifier for ECG Signal Processing

Theory/Description :

Electrocardiogram (ECG) signals have very small amplitudes and therefore require suitable analog front-end amplification before further signal processing. The proposed work reproduces a low-power CMOS folded electro-cascode amplifier reported for ECG applications.

The amplifier consists of MOSFET-based differential, current-mirror, folded-cascode and cascoded stages. The differential input stage senses the applied input signal and converts the input-voltage variation into a corresponding current variation. Current-mirror branches provide the required biasing, while the folded-cascode configuration directs the signal current toward the output stage and provides increased output resistance.

The reference circuit was designed for operation at low voltage and for low-power biomedical applications. In this Research Migration Project, the transistor-level circuit is reproduced using eSim and ngspice so that its electrical behaviour can be studied using an open-source simulation environment.

The reference publication reports implementation using 45-nm CMOS technology and Cadence Virtuoso.

Reason to reproduce with eSim :

The reference folded electro-cascode amplifier was originally designed and simulated using Cadence Virtuoso, which is a proprietary circuit-design environment. Reproducing the circuit in eSim provides an open-source implementation that can be studied and simulated without dependence on proprietary software.

Migration to eSim also provides educational value by allowing students and researchers to examine the transistor-level operation of the amplifier, perform different circuit analyses using ngspice, and compare the obtained behaviour with the published design.

The project therefore aims to demonstrate the reproducibility of a published CMOS biomedical amplifier using the open-source eSim environment and to provide a circuit that can be used for further learning and investigation.

Expected Outcome/outputs :

The expected outcome is a functional eSim implementation of the low-power CMOS folded electro-cascode amplifier reported in the selected research paper.

After completing the circuit in eSim, DC and transient analyses will be performed using ngspice. The expected outputs include the input and output voltage characteristics, DC transfer behaviour and transient response of the amplifier.

The simulation results will be used to verify the electrical operation of the migrated circuit and to compare its behaviour with the corresponding results reported in the reference publication.

Circuit Diagram:

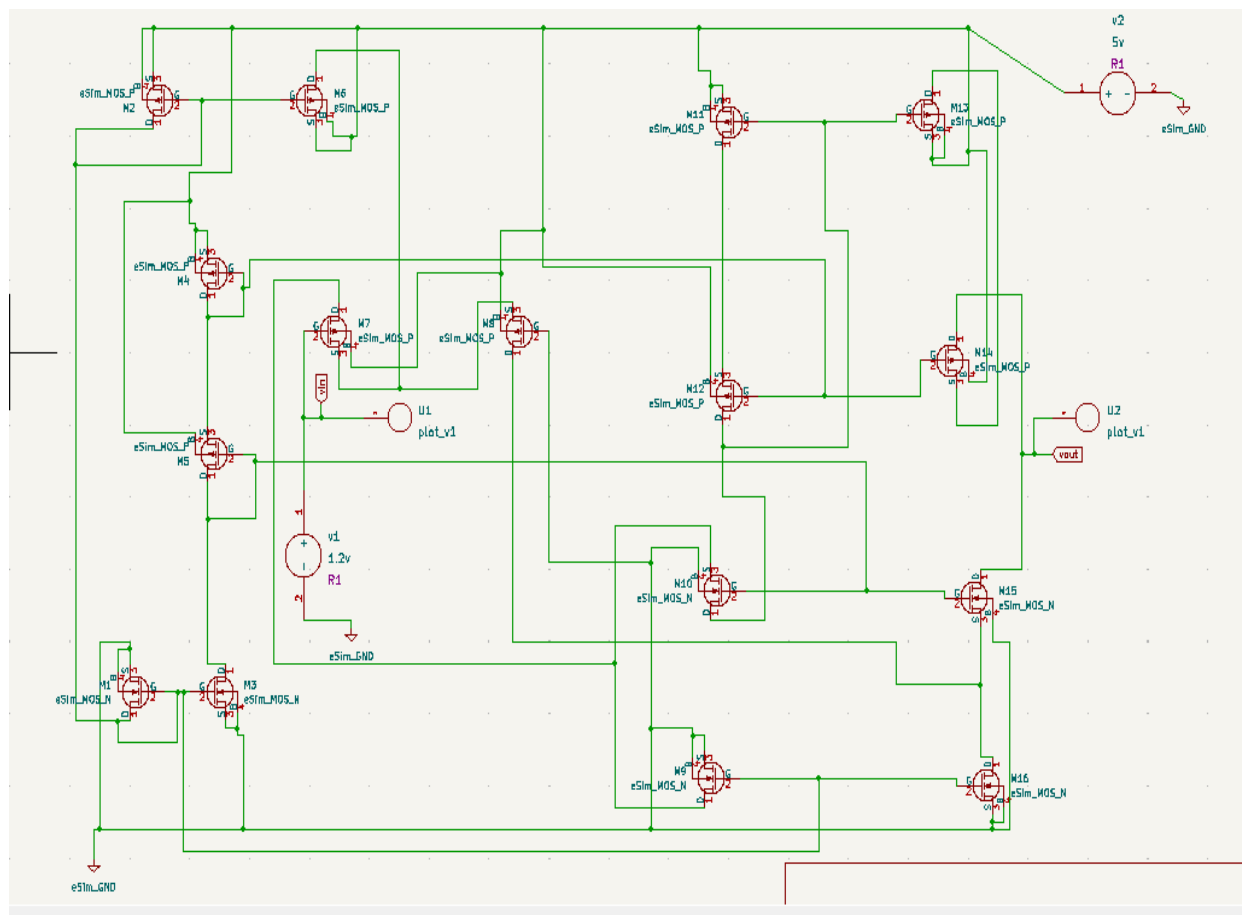
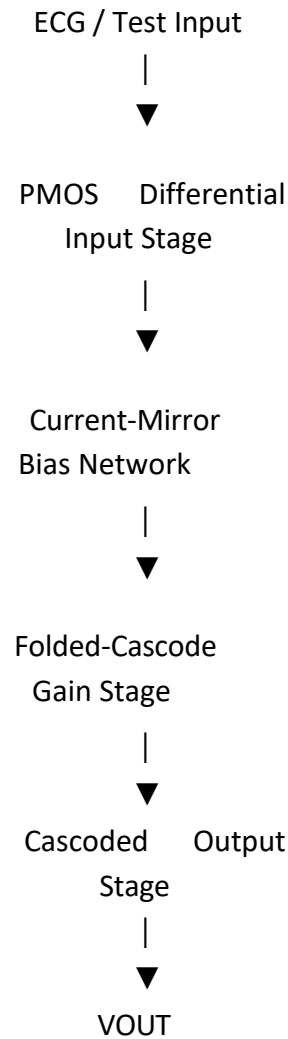


Figure 1. eSim implementation of the CMOS folded electro-cascode amplifier for ECG signal processing.

Block Diagram :



Expected Results (Input, Output waveforms and/or Multimeter readings):

The migrated circuit is expected to provide valid DC and transient responses when simulated using eSim/ngspice.

For DC analysis, the input voltage will be swept approximately from **0 V to 1.2 V**, and the corresponding output voltage will be observed. The present eSim simulation shows the output approaching approximately **5 V** as the swept input voltage increases.

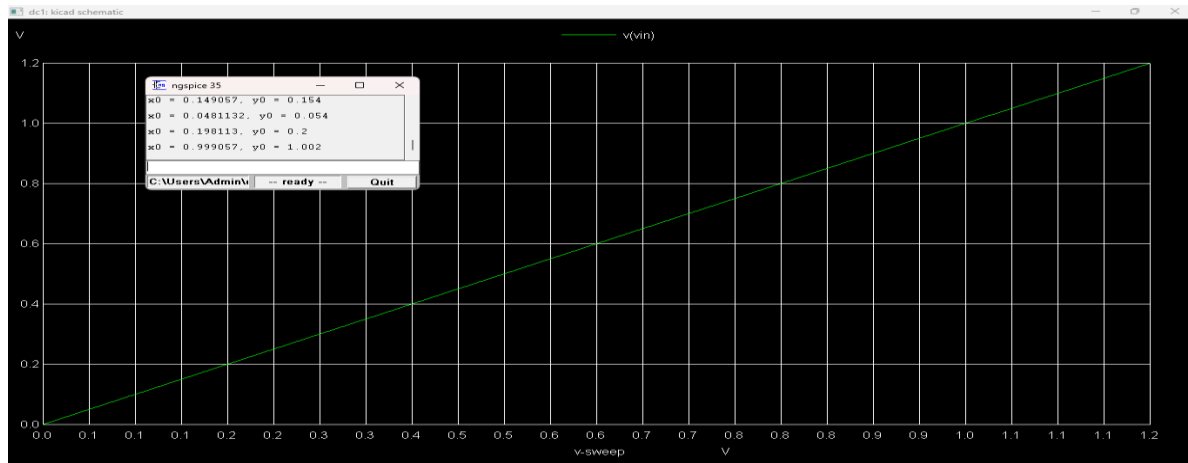
Representative values obtained from the present DC simulation include:

Input voltage, VIN Output voltage, VOUT

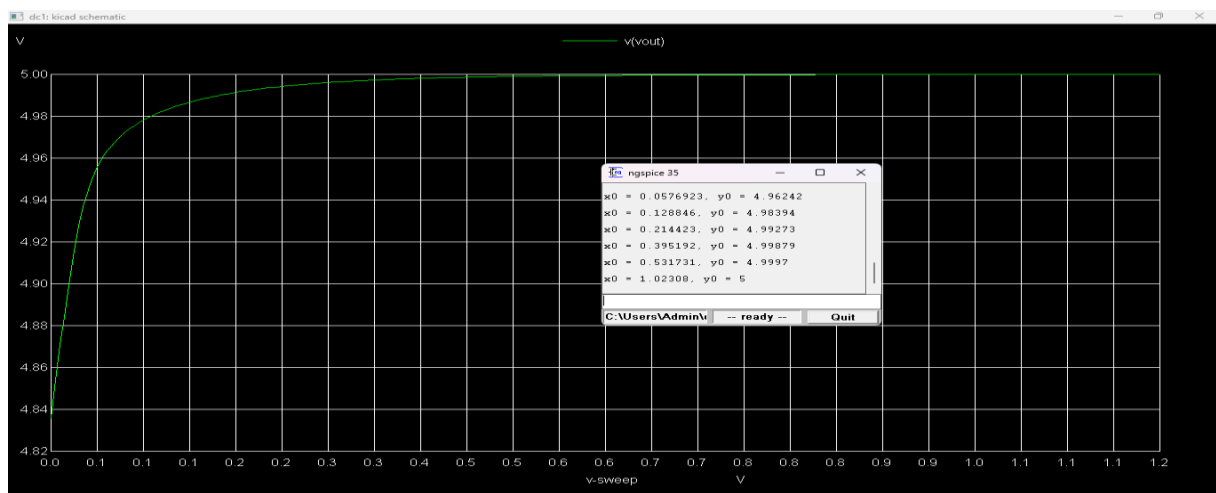
0.0577 V	4.9624 V
0.5317 V	4.9997 V
1.0231 V	approximately 5.000 V

The transient simulation will also be used to observe the input and output voltages with respect to time.

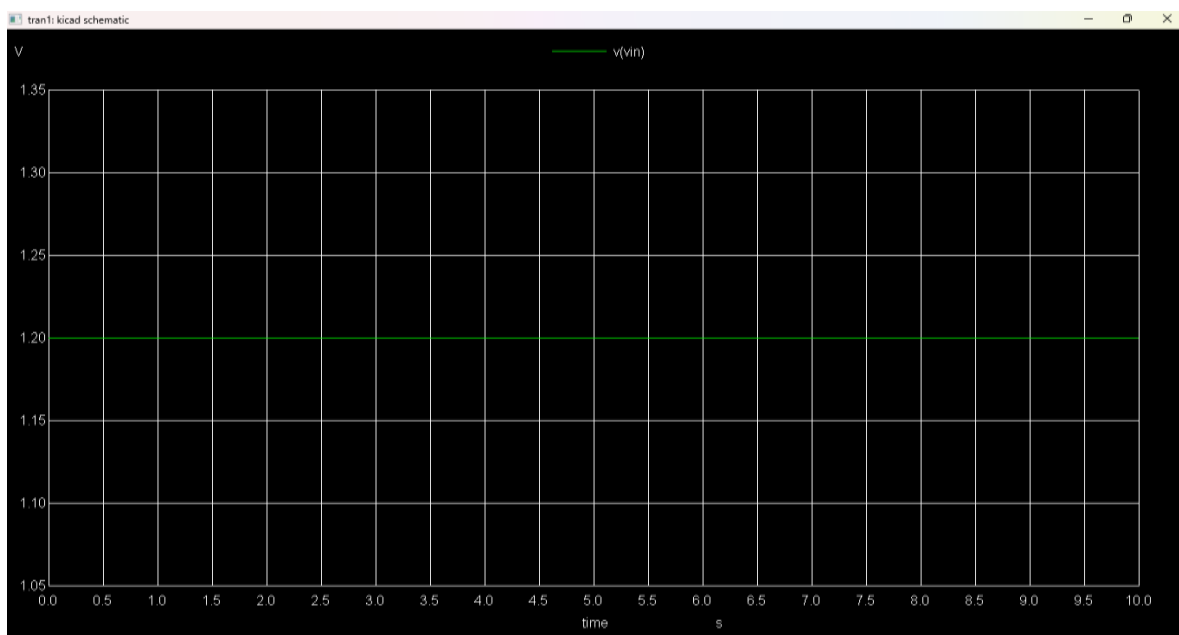
DC input sweep :



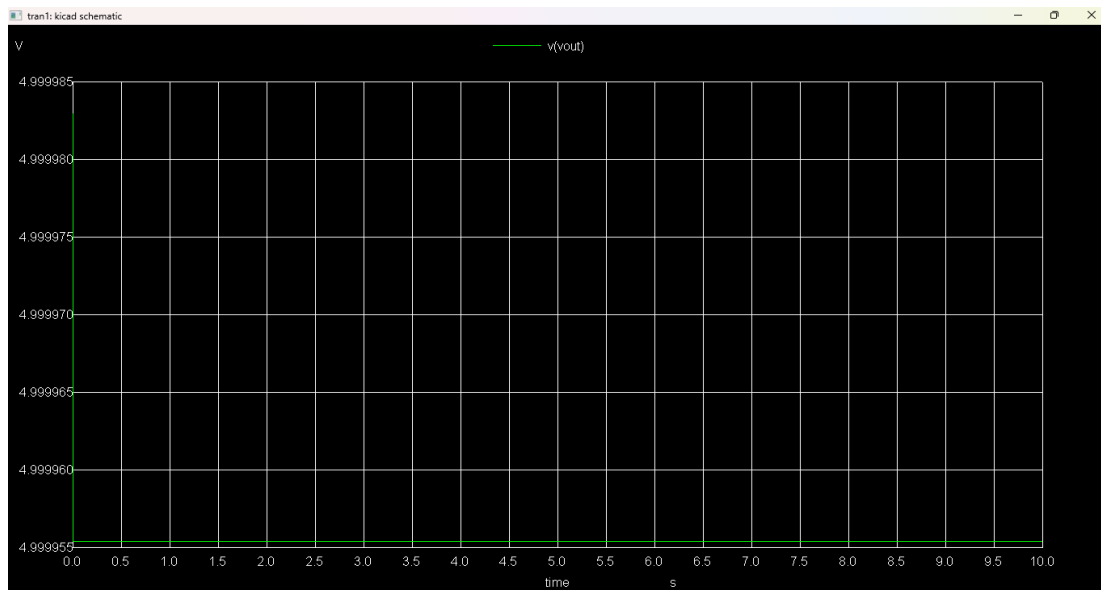
DC output response



Transient input response



Transient output response



Research Paper/Journal/etc. :

Title : Low Power CMOS Folded Electro Cascode Amplifier Design for Electrocardiogram Applications

Author :Rangeetha S; Ganesh Babu C; Bavana K B; Devadharshini M; Dharanya C.

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Link : <https://ieeexplore.ieee.org/document/11019942>

Source/Reference(s):

[1] S. Rangeetha, C. Ganesh Babu, K. B. Bavana, M. Devadharshini and C. Dharanya, “Low Power CMOS Folded Electro Cascode Amplifier Design for Electrocardiogram Applications,” *2025 Fourth International Conference on Smart Technologies, Communication & Robotics (STCR)*, IEEE, 2025, doi: 10.1109/STCR62650.2025.11019942.

[2] FOSSEE, IIT Bombay, *eSim – Research Migration Project*.

[3] eSim/ngspice, open-source circuit simulation environment used for implementation, simulation and waveform analysis