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Title of the circuit:

Simulation and Internal Circuit Analysis of the μ A740 FET-Input Operational Amplifier

Theory/Description:

The μ A740 is a monolithic, high-performance FET-input operational amplifier designed for analog applications that demand exceptionally high input impedance and extremely low input bias current. The architecture integrates Junction Field-Effect Transistors (JFETs) alongside bipolar junction transistors (BJTs) on a single integrated circuit. The input differential stage utilizes JFETs (Q6 and Q7) fed by constant current sources (Q1-Q3) and buffered by emitter followers to achieve minimal gate leakage current and extremely low input offset current, making it ideal for precision integrators, sample-and-hold circuits, and high-impedance sensor interfaces.

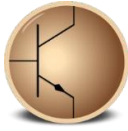
The internal structure consists of three main operational stages: the JFET differential input stage with active loading, a high-gain intermediate voltage amplification stage, and a push-pull class-AB output stage. Transistors Q10-Q16 form the active load and level-shifting network for the differential input pair, ensuring high common-mode rejection ratio (CMRR) and differential gain. An internal 50 pF frequency compensation capacitor (C1), connected in series with damping resistor R28, provides dominant-pole compensation directly within the chip to guarantee stable closed-loop operation across a wide range of gains without requiring external compensation components.

The output buffer section utilizes a complementary transistor configuration (Q31 and Q34) driven by intermediate driver circuitry (Q20-Q30). Current-limiting and short-circuit protection networks (R25, R29, and associated sensing transistors) guard the output stage against accidental overload or short circuits to ground or supply rails. Additionally, external offset-null pins (Pins 1 and 5) allow fine-tuning of the input offset voltage through an external potentiometer network connected directly to the active load resistors of the input stage.

Reason to reproduce with eSim:

The μ A740 is a specialized FET-input operational amplifier known for high input impedance and low bias current. Reproducing it in eSim expands the FOSSEE open-source library with an accurate simulation model for research and learning.

Recreating the complete transistor-level schematic rather than a basic macro-model lets users examine the exact inner workings of the JFET input, gain, and output stages. Verification ensures the sub-circuit matches datasheet specifications for reliable performance in open-source projects. Once validated, this model serves as a foundation for designing precision integrators, sample-and-hold circuits, and high-impedance sensor



interfaces. Access to internal nodes also enables clear academic analysis of internal frequency compensation and offset-nulling behavior. Ultimately, it offers a practical, accessible alternative to proprietary simulation software.

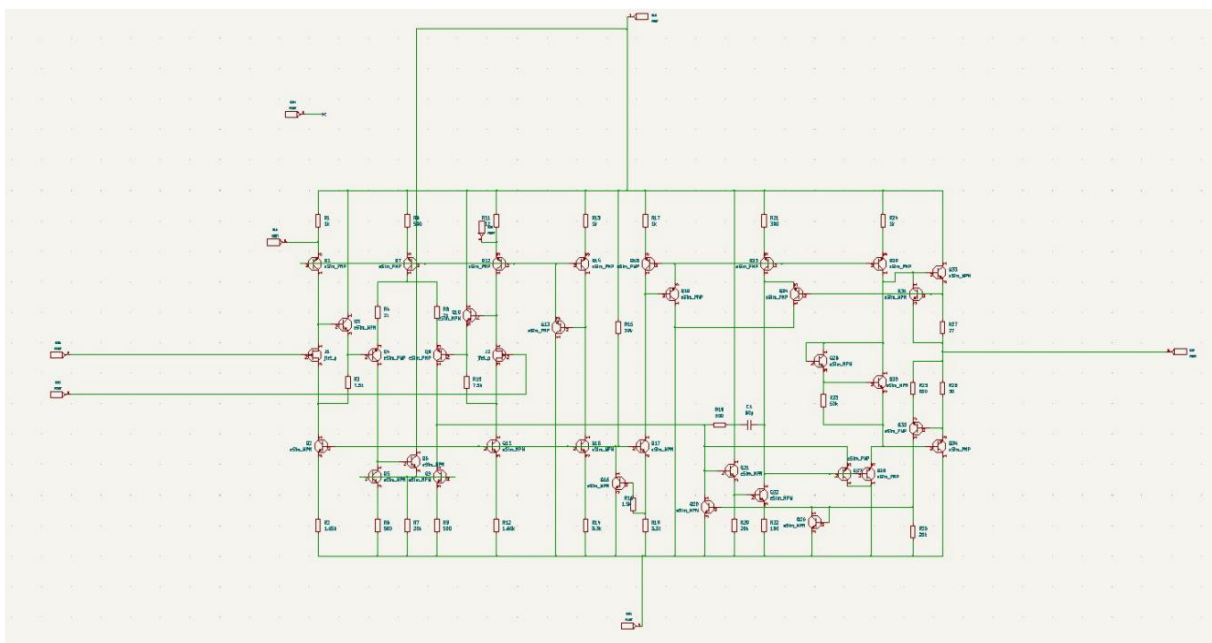
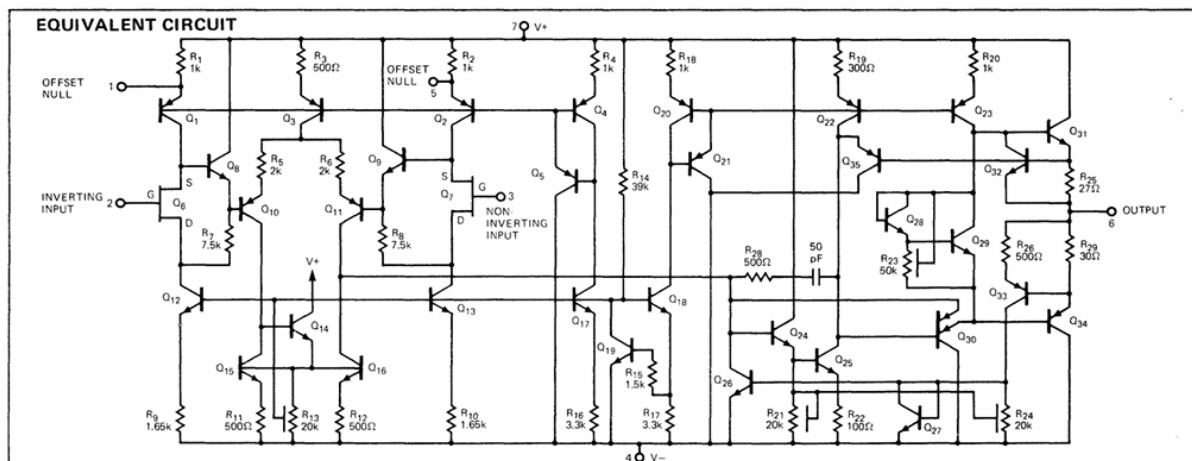
Expected Outcome/outputs:

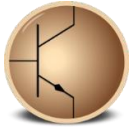
A fully functional, transistor-level uA740 FET-input operational amplifier model in eSim that accurately reproduces the behavior specified in the datasheet.

Validation performed by configuring the implemented amplifier as a unity-gain voltage follower to verify correct signal tracking, stability, and closed-loop operation.

Successful verification indicating that the uA740 model is suitable for deployment in other analog applications requiring high input impedance and low bias current.

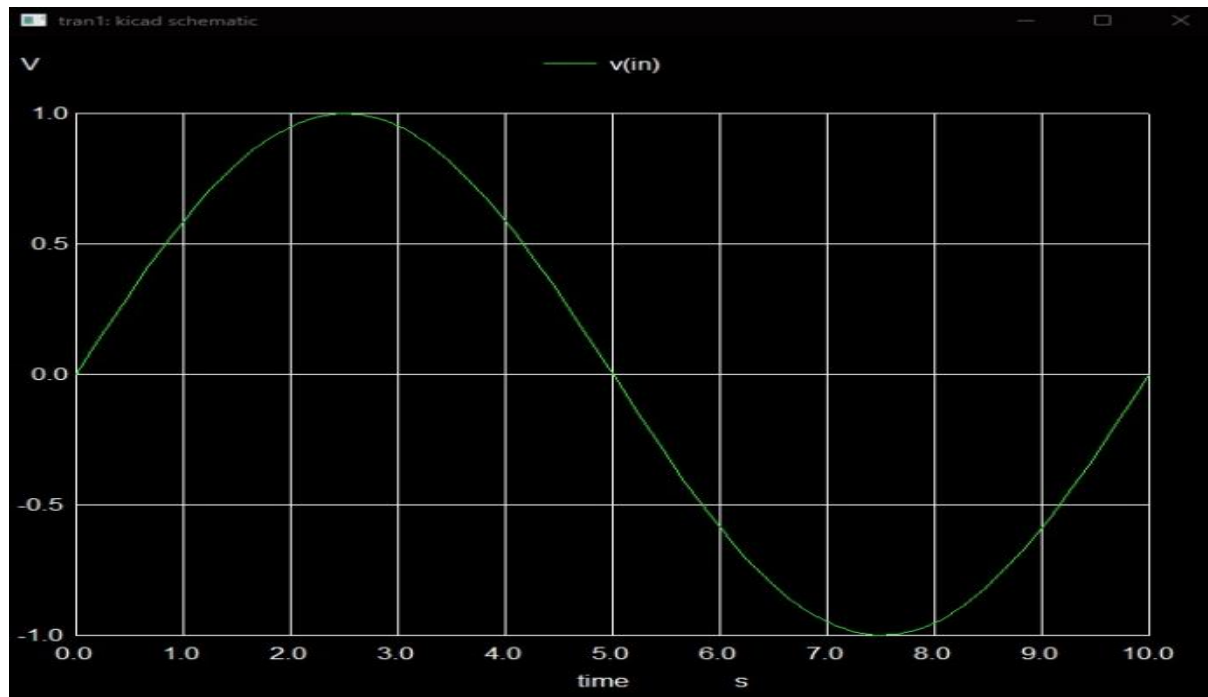
Circuit Diagram(s):



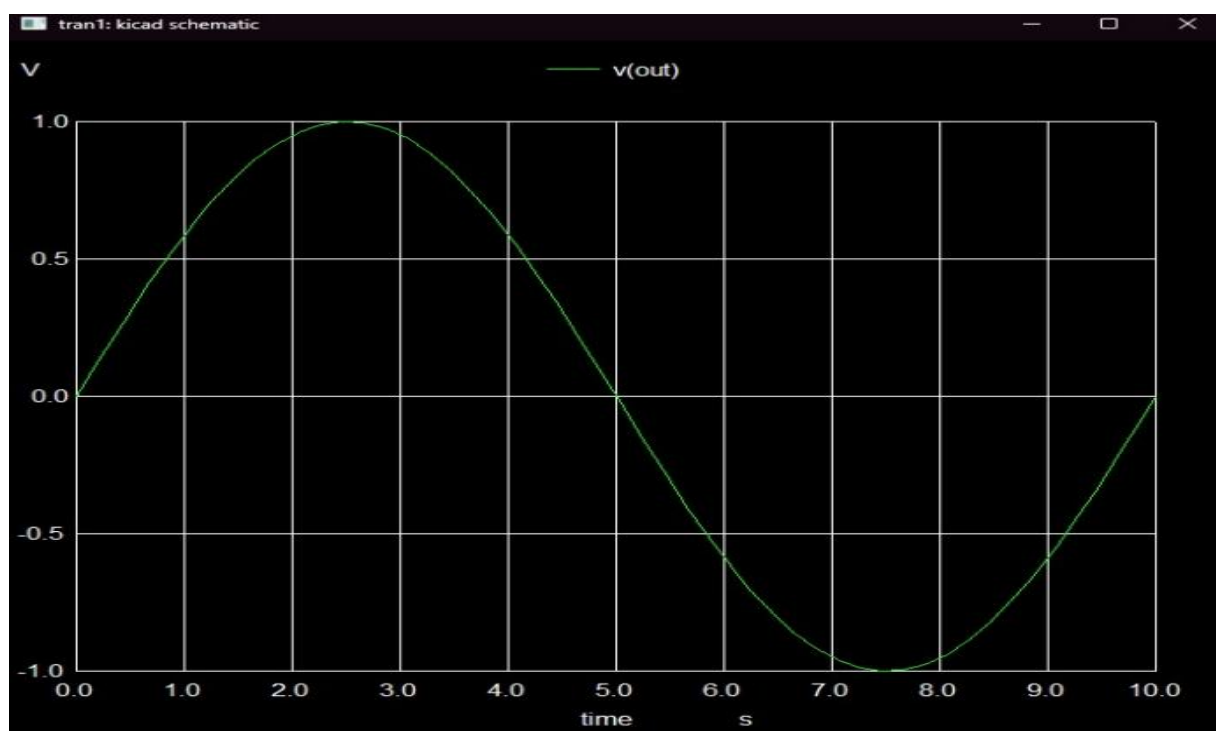


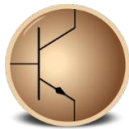
Expected Results (Input, Output waveforms):

Input Waveform:



Output Waveform:





Research Paper/Journal/etc.:

Title: μ A740 FET-Input Operational Amplifier Datasheet

Author: Fairchild Semiconductor / Texas Instruments

Page Number: Equivalent Circuit Section

Link: <https://www.ti.com/lit/ds/symlink/ua740.pdf>

Source/Reference(s):

1. Fairchild Semiconductor / Texas Instruments, μ A740 FET-Input Operational Amplifier Datasheet.
2. Sedra, A. S., C Smith, K. C., *Microelectronic Circuits*, Oxford University Press.
3. Boylestad, R. L., *Electronic Devices and Circuit Theory*, Pearson Education.
4. eSim Documentation, FOSSEE Project, IIT Bombay.