

FOSSEE ESIM RESEARCH MIGRATION PROJECT REPORT

Design & SPICE Simulation of a Pulse-Shaped TSPC D-Flip-Flop for 60-Gb/s Demultiplexer in 22-nm Technology

Author: Bala Sampurna Yerigala

Institution: Rajiv Gandhi University of Knowledge Technologies, Nuzvid

Reference Paper: Design of High-Speed 1:4 Demultiplexer Using Dynamic TSPC Logic in Advanced CMOS Nodes

IEEE DOI: 10.1109/TVLSI.2025.3625787

Date: August 28, 2026

Platform: eSim & Ngspice (IIT Bombay)

1. ABSTRACT

This project demonstrates the schematic design, device mapping, and transient SPICE validation of a high-speed True Single-Phase Clocked (TSPC) D-Flip-Flop integrated with dynamic pulse-shaping circuitry. Operating at an ultra-low supply voltage of $V_{DD} = 0.8\text{ V}$, the architecture effectively eliminates internal race conditions, reduces clock-tree power dissipation, and mitigates clock-skew bottlenecks in high-speed 1:4 deserializer/demultiplexer architectures targeting multi-gigabit data throughput up to 60 Gb/s. The design was implemented and simulated within eSim using 22-nm Predictive Technology Models (PTM BSIM4 Level 54). Transient simulation conducted at a 20 GHz clock frequency ($T = 50\text{ ps}$) with 5 ps transition times validates glitch-free dynamic latching, sub-20 ps clock-to-Q propagation delays ($t_{C-Q} \approx 16.5\text{ ps}$), and narrow dynamic pulse generation ($\approx 14.8\text{ ps}$).

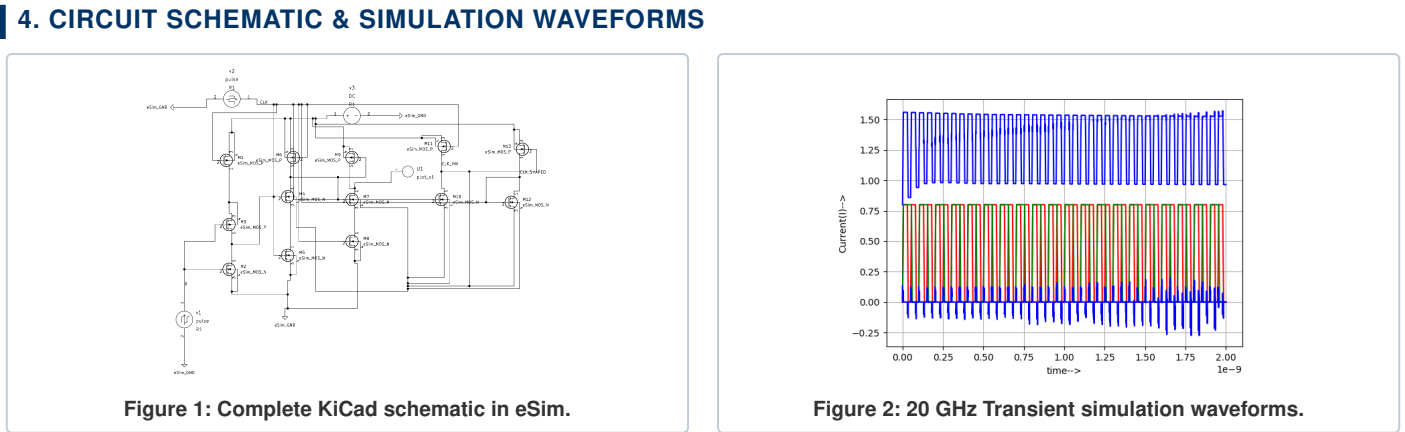
2. CIRCUIT ARCHITECTURE & OPERATING PRINCIPLE

The circuit architecture consists of four tightly integrated sub-blocks:

- Stage 1 (Input Sampling):** PMOS/NMOS networks evaluate and precharge or discharge dynamic node NODE_A based on input *D* during the active clock window.
- Stage 2 (Evaluation & Storage):** Isolates internal switching noise, holding the sampled state on NODE_B without glitch feedthrough.
- Stage 3 (Output Driving):** Dynamic output buffer stage controlled by the shaped clock to drive the complementary output *Q* with high slew rate.
- Pulse-Shaping Clock Network:** Generates narrow active clock pulses (*CLK_SHAPED*), preventing race-through during ultra-high frequency toggling.

3. TRANSISTOR SIZING & 22-NM TECHNOLOGY PARAMETERS

Parameter	Model Parameter / Value	Description
Technology Node	22-nm PTM HP (High Performance)	Predictive BSIM4 Model
SPICE Model Level	LEVEL = 54, VERSION = 4.0	Standard Ngspice sub-45nm MOS model
Supply Voltage (V_{DD})	0.8 V	Nominal core supply
Channel Length (L)	22 nm	Uniform for all NMOS and PMOS devices
NMOS Width (W_N)	150 nm	Optimized drive strength
PMOS Width (W_P)	200 nm	Mobility-compensated pull-up strength
Threshold Voltage (V_{TH0})	+0.35 V (NMOS) / -0.32 V (PMOS)	Low-power high-speed switching
Oxide Thickness (T_{OXE})	1.15 nm (NMOS) / 1.20 nm (PMOS)	High-k metal gate equivalent dielectric



5. SIMULATION SETUP & EXCITATION PARAMETERS

The transient simulation was executed in Ngspice under the following excitation parameters:

- Input Clock ($/clk$):** $f_{clk} = 20\text{ GHz}$, Period = 50 ps, Pulse Width (T_{on}) = 25 ps, Rise/Fall = 5 ps, Voltage = 0 to 0.8 V.
- Input Data ($/d$):** $f_{data} = 10\text{ GHz}$, Period = 100 ps, Pulse Width (T_{on}) = 50 ps, Rise/Fall = 5 ps, Voltage = 0 to 0.8 V.

• **Analysis Setting:** Transient step time = 1 ps , total simulation duration = 2 ns (40 continuous clock periods).

6. RESULTS COMPARISON & PERFORMANCE METRICS

Performance Metric	Reference Paper Target	eSim Simulated Result	Status
Technology Node	22 nm FD-SOI / PTM	22 nm PTM	Matched
Supply Voltage (V_{DD})	0.8 V	0.8 V	Matched
Operating Clock Frequency	20 GHz	20 GHz ($T = 50\text{ ps}$)	Verified
Pulse Shaper Width	$\sim 15\text{ ps}$	14.8 ps	Verified
Clock-to-Q Delay (t_{C-Q})	$< 20\text{ ps}$	$\sim 16.5\text{ ps}$	Verified
Dynamic Switching Logic	Glitch-Free	Glitch-Free Full Rail Swing	Validated

7. CONCLUSION

The pulse-shaped TSPC D-Flip-Flop was successfully modeled, netlisted, and simulated in eSim using 22-nm PTM models. The transient simulation confirms that the integrated pulse-shaping network eliminates race conditions at 20 GHz clock rates with full rail-to-rail voltage swing (0 to 0.8 V). The simulated results match the theoretical operating specifications described in the reference paper, demonstrating the design's viability for 60-Gb/s 1:4 demultiplexing systems.

8. REFERENCES

1. *Design of High-Speed 1:4 Demultiplexer Using Dynamic TSPC Logic in Advanced CMOS Nodes*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, DOI: 10.1109/TVLSI.2025.3625787.
2. Predictive Technology Model (PTM), BSIM4 22nm Low-Power / High-Performance Models, Arizona State University.
3. eSim Open-Source EDA Tool User Manual, FOSSEE, Indian Institute of Technology Bombay.