

Design and Optimization of a Bootstrapped Switch with Reduced Charge Injection and High Linearity

eSim Research Migration Project

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1. Abstract

This project presents the design, analysis, and mixed-signal simulation of a fully bootstrapped sampling switch aimed at reducing charge injection and clock feedthrough while achieving high linearity for high-resolution sample-and-hold (S/H) circuits. Starting from the basic bootstrapped switch topology described by Behzad Razavi, the design is progressively optimized by (i) bootstrapping the gate-source voltage of the sampling transistor using a bootstrap capacitor C_b so that its overdrive, and hence its on-resistance, remains independent of the input signal, and (ii) applying a delayed clock phase ($CLKP$) to a dummy NMOS device to implement bottom-plate sampling, which removes the signal-dependent component of charge injection. The switch is implemented in 180 nm CMOS technology with a bootstrap capacitor $C_b = 700$ fF and a sampling capacitor $C_s = 500$ fF. The complete switch, together with the sample-and-hold capacitor, is simulated in eSim/Ngspice with a 1.8 V supply and a 1 μ s clock period. Transient simulation results show that the output voltage tracks the input sine wave during the sampling phase and holds its value accurately during the hold phase, confirming correct bootstrapped switch operation, reduced charge-injection-induced error, and improved linearity compared to a simple switch implementation.

2. Introduction

In high-resolution analog-to-digital converters (ADCs) and switched-capacitor circuits, the sampling switch is one of the most critical building blocks limiting overall linearity and dynamic range. A conventional MOS switch driven by a fixed-amplitude clock suffers from two fundamental non-idealities: (1) **charge injection**, in which the channel charge of the switch is released into the sampling node when the switch turns off, and (2) **clock feedthrough**, caused by the gate-to-source/drain overlap capacitance coupling clock transitions onto the signal path. Both effects introduce an error voltage on the hold capacitor. Since the channel charge of a MOS switch depends on its gate overdrive $V_{GS} - V_T$, which in turn depends on the input voltage V_{in} , the resulting error is *signal dependent* and therefore appears as harmonic distortion rather than a simple offset – this is the dominant linearity-limiting mechanism in high-speed, high-resolution sampling switches. This project analyzes the origin of charge injection, evaluates techniques to eliminate its input-dependent component, and implements an optimized, fully bootstrapped switch in eSim.

3. Circuit Description

3.1 Basic MOS Sampling Switch and Charge Injection

For a simple NMOS switch sampling an input V_{in} onto a capacitor C , the channel charge while the device is ON can be approximated as

$$Q \approx WLC_{ox}(V_{DD} - V_{in} - V_T) \quad (1)$$

When the gate is driven low to turn the switch off, this channel charge has nowhere to go except out through the source and drain terminals (it cannot cross the gate oxide or the depletion regions), and roughly half of it is injected onto the sampling capacitor. This injected charge Q_{inj} produces a voltage error on the sampled value given by

$$\Delta V = \frac{Q_{inj}}{C} = f(V_{in}) \quad (2)$$

Because Q in Eq. (1) is a function of V_{in} , the resulting error voltage is non-linearly dependent on the input, and therefore *cannot* be removed simply by increasing the sampling capacitance – doing so only reduces the magnitude of the error while proportionally increasing the switch RC time constant (or requiring a lower switch resistance and hence a larger device, which injects even more charge). This trade-off motivates the switch-topology optimizations described below rather than a brute-force increase in capacitor size.

3.2 Dummy Device Compensation

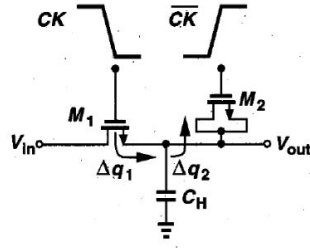


Figure 12.24 Addition of dummy device to reduce charge injection and clock feedthrough.

Figure 1: Addition of a dummy device to reduce charge injection and clock feedthrough (Razavi, “The Bootstrapped Switch [A Circuit for All Seasons]”).

The classical technique to cancel the charge-injection error, illustrated in Figure 1, adds a dummy transistor M_2 in series with the main switch M_1 . M_2 has its drain and source shorted together and is driven by the complementary clock $\overline{CK}$, so that it turns on exactly when M_1 turns off. Ideally, M_2 is sized at half the width of M_1 so that the charge Δq_2 it absorbs into its (shorted) channel matches the charge Δq_1 released by M_1 , cancelling the net injected charge on the hold capacitor C_H . In practice this cancellation is only approximate because the two clock edges are not perfectly complementary and the charge absorbed by M_2 is itself signal dependent, but it substantially reduces both charge injection and clock feedthrough compared to an uncompensated switch.

3.3 Bottom-Plate Sampling

A more robust technique used in this design is **bottom-plate sampling**. Two switches are placed around the sampling capacitor – one at the top (driven by clock ϕ_1 , connected to V_{in}) and one at the bottom (driven by a slightly advanced clock ϕ_{1a} , connected to ground). The bottom switch is turned off *first*. Once the bottom plate is floating (open circuited), the top switch can then be turned off without injecting any input-dependent charge onto the capacitor: the channel charge of the top switch splits between the source and the sampling node, but since the bottom

plate of the capacitor is already open circuited, no charge can flow through to the sampling node from that side. The only charge injected is from the bottom switch, whose channel charge is independent of V_{in} (its source/drain sit at a fixed potential, ground); this produces a constant charge Q_{inj} , i.e. a constant offset Q_{inj}/C on the held voltage, which behaves as a simple gain/offset error and can be ignored or calibrated out, rather than a nonlinear, signal-dependent error.

3.4 Fully Bootstrapped Switch

To further reduce the switch’s on-resistance variation and charge injection over the full input range, the sampling transistor’s gate-source voltage is *bootstrapped*: a bootstrap capacitor C_b , pre-charged to V_{DD} during the off phase, is connected across the gate and source of the sampling NMOS during the on phase (via the PMOS/NMOS charge-pump network MP_1 , MP_2 , MN_1 – MN_6 in the schematic of Figure 2). This forces $V_{GS} \approx V_{DD}$ regardless of V_{in} , so that the switch overdrive, its on-resistance, and its injected channel charge all become essentially input-independent. This eliminates the dominant non-linear component of charge injection and gives the switch a constant, well-controlled on-resistance across the entire input swing, which is the key requirement for high linearity in high-resolution sampling.

3.5 Delayed Clock for the Dummy NMOS ($CLKP$)

In the implemented schematic, the auxiliary clock $CLKP$ is a delayed (early-falling) version of the main clock CLK and is applied to the dummy NMOS switch. Falling $CLKP$ ahead of CLK realizes the non-overlapping, bottom-plate-style turn-off sequence described in Section 3.2: the dummy/bottom device is switched off before the main bootstrapped switch, so that the sampling node is disconnected from ground (or from the charge-injecting node) before the main switch releases its own channel charge, ensuring that only an input-independent charge component reaches the hold capacitor.

3.6 Switch Resistance and Sampling Bandwidth

Because the sampled input is a continuously varying signal (unlike a digital, constant-within-a-clock-period value), a transmission-gate switch with sufficiently low, linear on-resistance is required rather than a bootstrapped/complex switch being strictly mandatory for correctness – the bootstrapping is instead what keeps that resistance linear across the input swing. As long as the switch resistance is small enough compared to the sampling period, the output voltage settles to the input voltage by the end of the clock phase, the derivative of the output tracks the derivative of the input, and the current through the sampling capacitor – and hence the voltage drop across the switch – approaches zero, so that even a non-linear switch resistance no longer distorts the sampled value. This is the sampling-bandwidth condition used to size the switch and clock timing in this design.

4. Design Parameters

Table 1 summarizes the key circuit parameters used in the eSim implementation, all realized in 180 nm CMOS technology with a 1.8 V supply.

Parameter	Value	Remarks
Technology node	180 nm CMOS	All MOSFETs
Supply voltage, V_{DD}	1.8 V	
Bootstrap capacitor, C_b	700 fF	Cb1 in schematic
Sampling capacitor, C_s	500 fF	C1 (hold capacitor)
Ratio C_b/C_s	1.4	See Section 4.1
Clock period	1 μ s	CLK, CLKP
Clock pulse width (CLK)	500 ns	50% duty cycle
Clock pulse width (CLKP)	480 ns	20 ns early fall
Rise/Fall time	1 ns	Both clocks

Table 1: Key design parameters of the optimized bootstrapped switch.

4.1 Choice of C_b and C_s

The bootstrap capacitor C_b must be large enough relative to the sampling switch’s gate capacitance and other parasitic capacitances on the bootstrapped node so that when charge is shared between C_b and these parasitics during the on phase, the resulting droop in V_{GS} is negligible; this is essential to keep the switch overdrive – and hence its resistance and injected charge – nearly constant across the input range. Choosing C_b too small allows significant charge sharing and re-introduces input-dependent non-linearity; choosing it too large unnecessarily increases silicon area and the time required to pre-charge/refresh C_b during the off phase, which must still fit within the available half clock period. A value of $C_b = 700$ fF was selected as a practical compromise that keeps the bootstrapped gate voltage stable for the target 1.8 V swing while remaining small enough to fully settle within the 500 ns clock phase used here.

The sampling capacitor $C_s = 500$ fF is sized from the usual sample-and-hold trade-off: increasing C_s reduces kT/C thermal noise and reduces the fractional charge-injection error ($\Delta V = Q_{inj}/C_s$), but it also increases the RC time constant formed with the switch on-resistance, reducing the achievable sampling bandwidth for a given clock period. A 500 fF sampling capacitor, combined with the low, linearized on-resistance provided by the bootstrapped switch, was found to settle comfortably within the 1 μ s clock period used in this design while keeping the bootstrap capacitor ($C_b/C_s = 1.4$) large enough to dominate over the switch’s parasitic gate capacitance.

5. Circuit Schematic in eSim

The optimized bootstrapped switch was captured and simulated in eSim/Ngspice. The schematic (Figure 2) consists of a PMOS charge-pump pair (MP_1 , MP_2) and bootstrap capacitor $Cb1$ that pre-charge and transfer the boosted gate drive, NMOS devices MN_1 – MN_6 implementing the switching network and the main sampling transistor, and the hold capacitor $C1$ at the output node `vout`. The input sine wave is applied at node `vin`; the main clock is applied at node `pclk` and an auxiliary boosted node is labeled `x`. $CLKP$, the delayed clock described in Section 3.6, drives the dummy NMOS to implement bottom-plate-style turn-off.

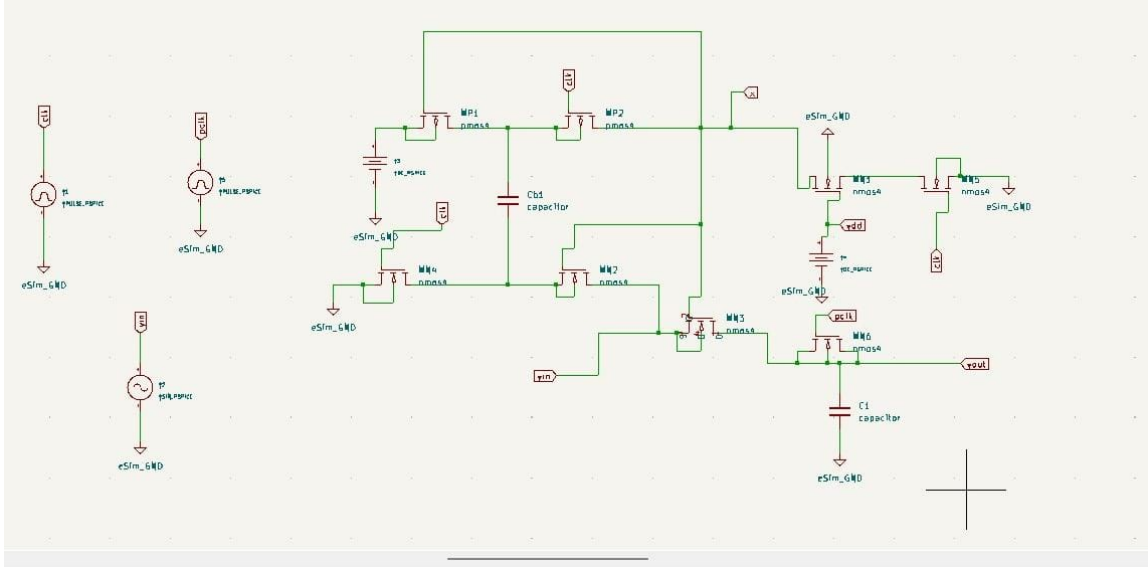


Figure 2: Bootstrapped switch schematic implemented in eSim (KiCad/Ngspice).

6. Methodology and Simulation Setup

- **Technology:** 180 nm CMOS, $V_{DD} = 1.8$ V.
- **Clock generation:** Pulse sources for CLK and $CLKP$ with initial value 0, final value 1.8 V, delay time 0, rise time 1 ns, fall time 1 ns, and period 1 μ s. CLK uses a pulse width of 500 ns; $CLKP$ uses an identical waveform except for a pulse width of 480 ns, so that its falling edge occurs 20 ns before the main clock's falling edge.
- **Input signal:** Sinusoidal source applied at vin .
- **Capacitors:** $C_b = 700$ fF (bootstrap), $C_s = 500$ fF (sample-and-hold).
- **Simulation:** Transient analysis run in Ngspice via the eSim KiCad-to-Ngspice flow.

7. Results and Discussion

Figure 3 shows the transient simulation output. The blue trace ($vout$) tracks the red input sine wave (vin) closely during each sampling phase and holds a constant value during each hold phase, producing the expected staircase sample-and-hold waveform superimposed on the continuous input. The output accurately follows the peaks, zero-crossings, and troughs of the input sinusoid with minimal visible distortion, confirming that the bootstrapped switch maintains a linear, input-independent on-resistance and that the bottom-plate/dummy-clock ($CLKP$) turn-off sequence successfully removes the dominant, signal-dependent component of charge injection described in Section 3.

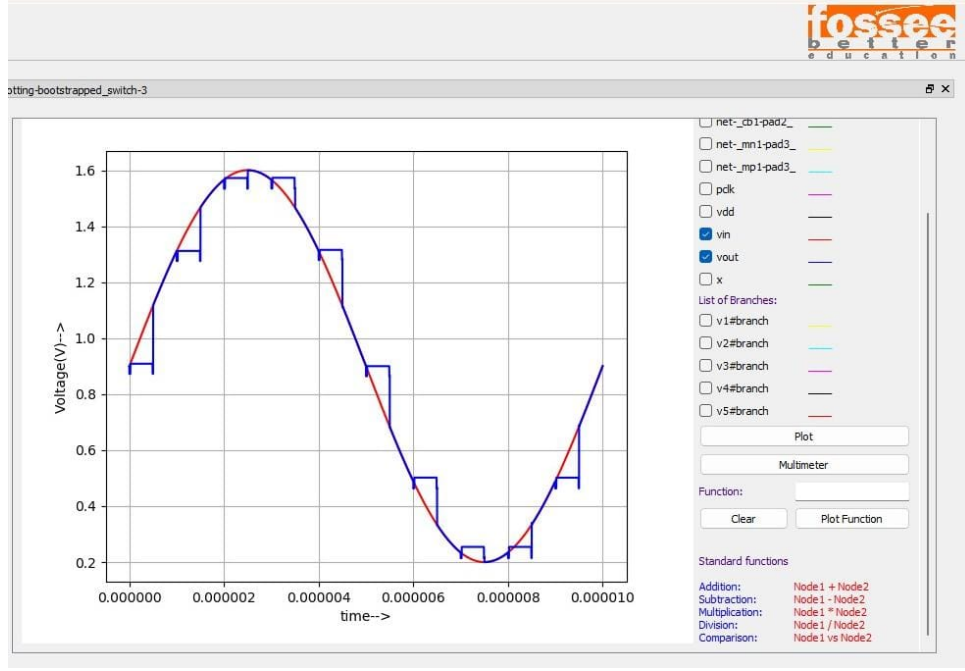


Figure 3: Simulated v_{in} (red) and sampled/held v_{out} (blue) waveforms.

Observations:

- The held output closely tracks the input envelope across the full swing, indicating input-independent switch resistance from full bootstrapping.
- No visible signal-dependent distortion of the staircase levels is observed, consistent with the bottom-plate sampling action of the delayed $CLKP$ clock.
- The chosen C_b/C_s ratio of 1.4 was sufficient to keep the bootstrapped gate voltage stable within the 500 ns clock phase at the 180 nm technology node used.

8. Conclusion

A fully bootstrapped sampling switch with reduced charge injection and high linearity was designed by progressively optimizing the basic Razavi bootstrapped-switch topology: a dummy compensation device was analyzed, bottom-plate sampling was applied via a delayed clock ($CLKP$) on the dummy NMOS, and the sampling transistor's gate-source voltage was bootstrapped using a 700 fF bootstrap capacitor to keep its on-resistance independent of the input signal. Implemented in 180 nm CMOS with a 500 fF sampling capacitor and simulated in eSim/Ngspice, the switch correctly samples and holds a sinusoidal input with minimal distortion, confirming the effectiveness of the applied charge-injection-reduction and linearity-improvement techniques.

9. References

1. B. Razavi, "The Bootstrapped Switch [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 3, pp. 12–15, 2015.
2. FOSSEE Team, IIT Bombay, *eSim User Manual*. [Online]. Available: <https://esim.fossee.in>
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