

# Research Migration Project

<https://esim.fossee.in/research-migration-project>



The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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**Title of the circuit :** Edge Detector Circuit to Detect the Presence of Processor Clock

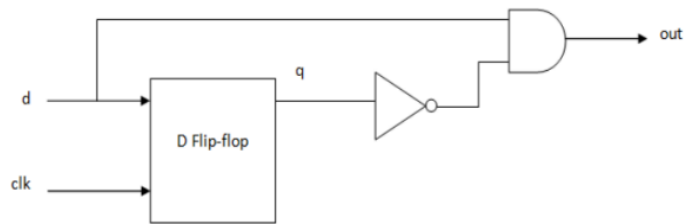
**Theory/Description :** An edge detector circuit is used to detect the rising edge of an input clock signal. The circuit uses a D flip-flop, NOT gate, and AND gate. The D flip-flop provides a delayed signal, which is inverted and combined with the input signal using the AND gate. A short output pulse is generated when a rising edge occurs, indicating the presence of the processor clock.

**Expected Outcome/outputs :**

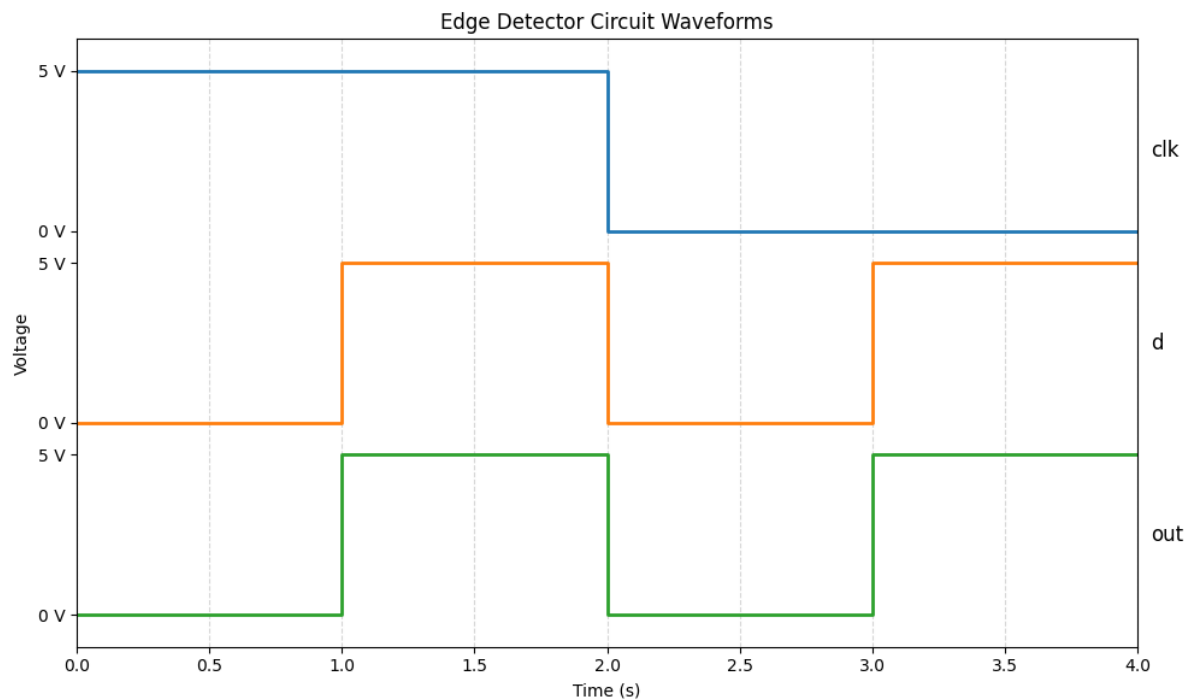
| clk | d | out |
|-----|---|-----|
| 1   | 0 | 0   |
| 1   | 1 | 1   |
| 0   | 0 | 0   |
| 0   | 1 | 1   |

The circuit is expected to detect the rising edge of the processor clock and generate a short output pulse. The input and output waveforms will be observed using transient analysis in eSim. The output pulse will indicate the presence of the processor clock.

### Circuit Diagram(s) :



### Expected Results (Input, Output waveforms and/or Multimeter readings) :



### Research Paper/Journal/etc. :

**Title :** FPGA Based Clock Frequency Sensor and Range Estimating System for Testing Memories and Processors

**Author :** C. Manjula and D. Jayadevappa

**Page No. :** 11–21

**Link :**

[https://scholar.google.com/citations?view\\_op=view\\_citation&hl=en&user=UQ0Z4m4AAAAJ&citation\\_for\\_view=UQ0Z4m4AAAAJ:9yKSN-GCB0IC](https://scholar.google.com/citations?view_op=view_citation&hl=en&user=UQ0Z4m4AAAAJ&citation_for_view=UQ0Z4m4AAAAJ:9yKSN-GCB0IC)