

Edge Detector Circuit to Detect the Presence of Processor Clock

Amrutha M
Electronics and Communication
Engineering
Cochin University of Science and
Technology
Kochi, Kerala

Abstract— This project implements an Edge Detector Circuit to detect the presence of a processor clock. The circuit uses a D flip-flop, NOT gate, and AND gate to detect the rising edge of an input clock signal. When a rising edge occurs, the circuit produces a short output pulse. The circuit is designed and tested using eSim simulation.

Keywords— Edge Detector, D Flip-Flop, Rising Edge, Processor Clock

I. INTRODUCTION

An Edge Detector Circuit is used to detect a change in a digital signal. In this project, the circuit is used to detect the rising edge of a processor clock. The circuit uses a D flip-flop, NOT gate, and AND gate. When the clock signal has a rising edge, a short pulse is produced at the output. This pulse confirms the presence of the processor clock.

II. OBJECTIVES

The aim of this project is to design an edge detector circuit that detects the rising edge of a processor clock signal and produces a short output pulse. The project focuses on implementing the circuit using a D flip-flop, NOT gate, and AND gate. The goal is to build the truth table, perform transient analysis simulation, and verify that the circuit correctly detects the presence of the processor clock signal.

III. IMPLEMENTATION

The edge detector circuit is made using a D flip-flop, NOT gate, and AND gate. The input signal is given to the D flip-flop. The output of the flip-flop is inverted using a NOT gate. The input signal and the inverted flip-flop output are then given to the AND gate. When a rising edge occurs, the output becomes HIGH for a short time. This short pulse indicates the presence of the processor clock.

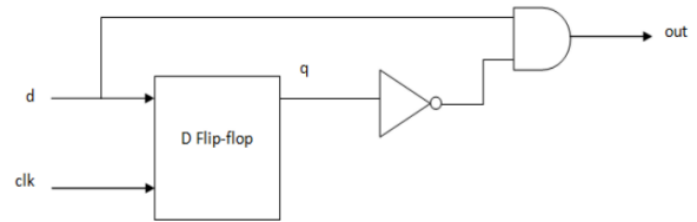


Fig. 2. Logic Diagram

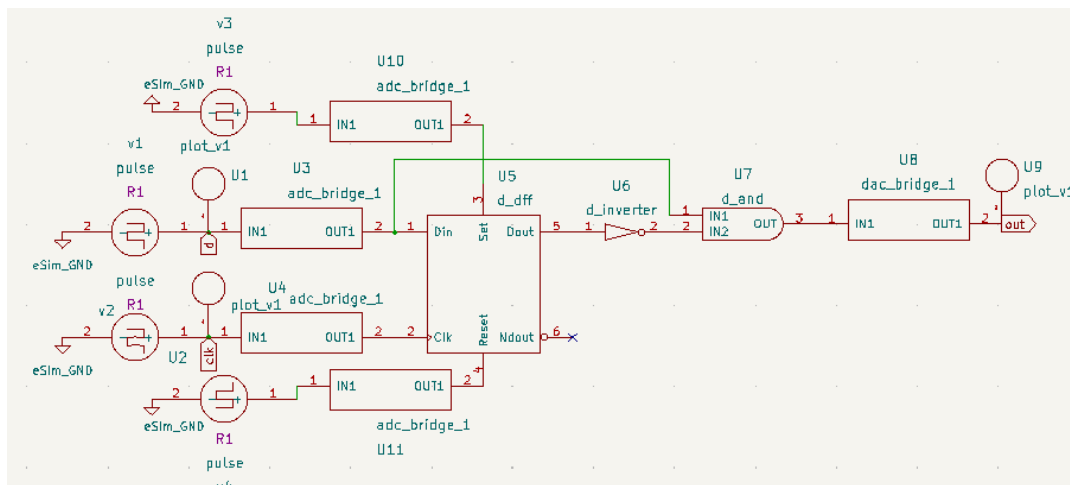


Fig. 1. eSim Circuit Schematic

IV. RESULTS

The edge detector circuit was implemented and tested using eSim. Different clock and input signals were applied to the circuit. The output waveform was observed using transient analysis.

The simulation showed that the circuit produces a short output pulse when a rising edge is detected. This confirms that the circuit can be used to detect the presence of a processor clock.

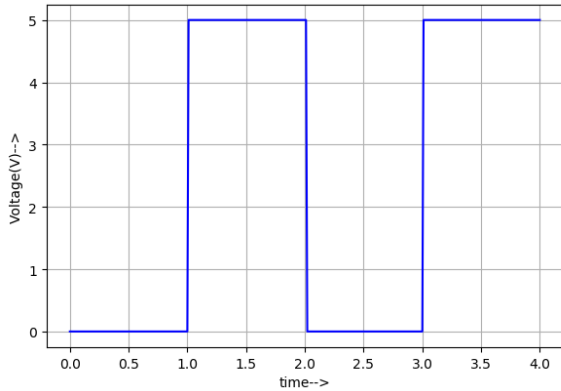


Fig. 3. Input d

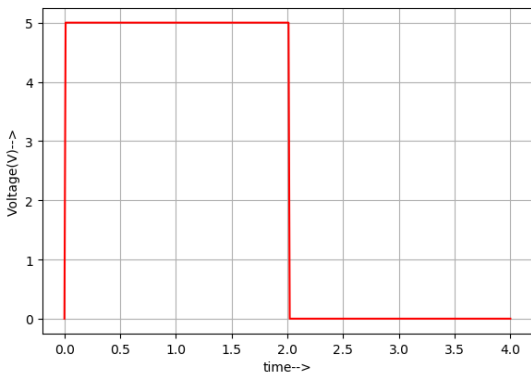


Fig. 4. Input clk

Figures 3 and 4 represent the 2 inputs d and clk.

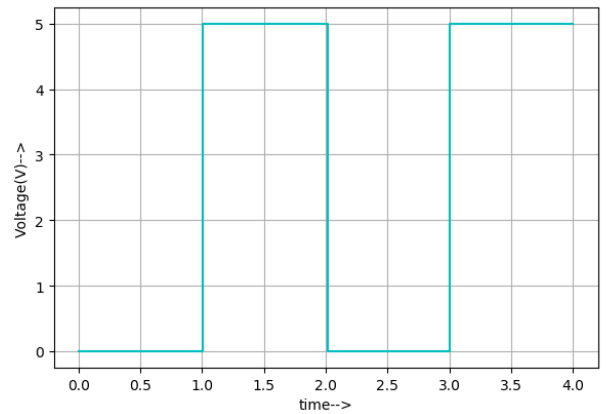


Fig. 5. Output out

Figures 5 represents the output.

V. ANALYSIS

The circuit was verified using transient analysis. The input clk and d signals were applied to the circuit, and the output was observed. The output pulse occurred when the required rising edge was detected. The simulation results matched the expected operation of the edge detector circuit.

VI. CONCLUSION

The Edge Detector Circuit was successfully designed and simulated using eSim. The circuit uses a D flip-flop, NOT gate, and AND gate to detect the rising edge of a processor clock. The transient analysis confirmed that a short output pulse is generated when the clock edge is detected. Therefore, the circuit can be used to detect the presence of clock signals in digital systems.

REFERENCES

Manjula, C., & Jayadevappa, D. (2020). *FPGA based clock frequency sensor and range estimating system for testing memories and processors*. International Journal of Electrical Engineering and Technology (IJEET), 11(5), 11–21.