

Low-Power SR Flip-Flop Design with ONOFIC Implementation Using eSim

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Problem Statement:

Develop a low-power SR flip-flop circuit to reduce leakage current and static power dissipation, addressing the challenges of power consumption in modern CMOS-based VLSI design. The solution focuses on using the ONOFIC (ON/OFF) technique for enhanced performance.

Theory/Description:

This study presents the design and simulation of a soft-error-aware SRAM with multinode upset tolerance for aerospace applications. By incorporating advanced error correction codes (ECCs) and redundancy, the design detects and corrects multinode errors efficiently. Simulations validate its high reliability and low power consumption, ensuring stable operation in radiation-prone environments.

Circuit Diagram:

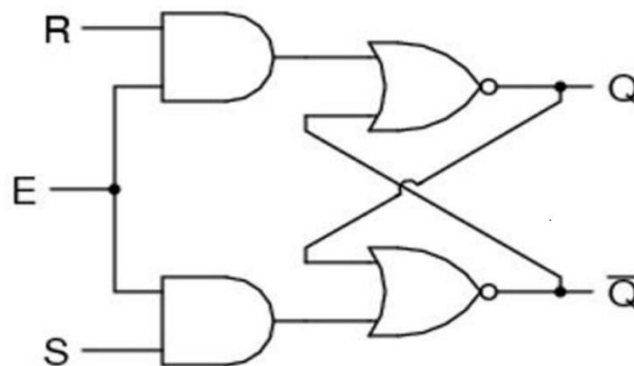


Fig.1 NOR based SR flip-flop

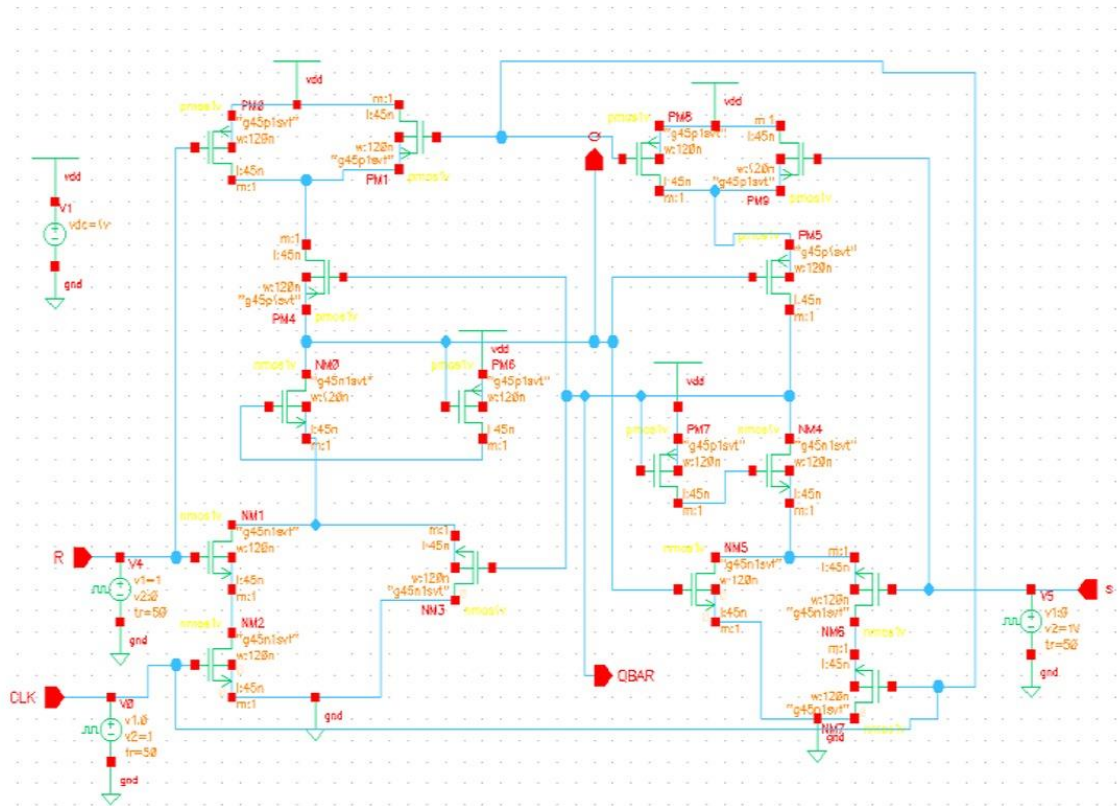


Fig.2 ONOFIC implementation of CMOS SR flip-flop

Reference: Malik, Masood Ahmad, and Vijay Kumar Sharma. "Design of low power SR-flip-flop with on/off (ONOFIC) implementation." *2019 International Conference on Communication and Electronics Systems (ICCES)*. IEEE, 2019.

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Simulation Output:

