

Design, Verification, and Comparative Power Evaluation of an RS(15, 11) Reed-Solomon Encoder using Operand Isolation

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Abstract—Reed-Solomon RS(15, 11) is a non-binary cyclic forward error-correcting (FEC) block code that is highly effective in modern communication systems. However, the continuous switching of internal Galois Field multiplier trees across all clock cycles leads to excessive dynamic power dissipation. This paper presents the design, verification, and comparative power evaluation of a standard baseline RS(15, 11) encoder and an optimized architecture utilizing operand isolation. The design is implemented and verified using the open-source eSim toolchain, integrating NgVeri and Ngspice. Co-simulation results demonstrate 100% functional equivalence and zero latency penalty, while the optimized architecture achieves a 73.33% reduction in multiplier switching activity, significantly reducing internal dynamic power.

Index Terms—Reed-Solomon, Forward Error Correction, Operand Isolation, eSim, Low Power Design, Galois Field.

I. INTRODUCTION

Addition and polynomial multiplication are fundamental operations in digital communication systems, forming the backbone of forward error-correcting (FEC) mechanisms. The Reed-Solomon RS(15, 11) code is a widely adopted non-binary cyclic FEC block code operating over Galois Field arithmetic, $GF(2^m)$. In standard implementations, the circuit processes an 11-symbol input message sequence and computes 4 parity check symbols to construct a 15-symbol systematic codeword via a Linear Feedback Shift Register (LFSR) architecture.

While traditional LFSR datapaths are mathematically robust, their internal Galois Field multiplier trees and XOR feedback networks switch continuously across all 15 clock cycles. This unrestricted toggling wastes dynamic power, especially during the message streaming phase when feedback parity computation is not immediately required at the output.

Approximate computing and dynamic power management techniques exploit algorithmic idle phases to improve energy efficiency. By incorporating operand isolation (input gating), multiplier inputs can be held static during the initial 11-cycle message transmission phase, activating the feedback multiplier logic exclusively during the final 4 parity computation cycles. This paper focuses on evaluating this low-power methodology using an open-source mixed-signal EDA workflow.

II. IMPLEMENTATION IN ESIM

The RS(15, 11) encoders were modeled using Verilog HDL and integrated into the eSim environment using the NgVeri module. eSim provides a unified open-source workflow that bridges KiCad schematic capture and the Ngspice simulation engine, eliminating the dependency on proprietary commercial EDA suites.

The design incorporates two distinct structural implementations co-simulated under identical clock, reset, and data stimuli:

- **Baseline Architecture (`rs_encoder_baseline`):** A standard LFSR datapath lacking input gating.
- **Isolated Architecture (`rs_encoder_isolated`):** Incorporates operand isolation to freeze Galois Field multiplier inputs to zero during the message phase.

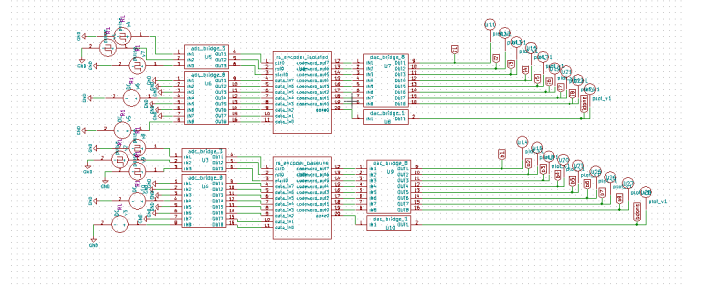


Fig. 1. schematic implemented in esim

Simultaneous instantiations of the baseline and optimized digital architectures were placed within a single KiCad testbench. XSPICE mixed-signal interface bridges, specifically `adc_bridge_8` and `dac_bridge_8`, were utilized to interface the digital Verilog boundaries with analog high-speed pulse and DC excitation sources.

III. VERIFICATION

Verification was conducted by establishing direct waveform and timing comparisons through Ngspice transient analysis. A 10 ns clock period (100 MHz) was applied alongside synchronized reset and start pulses. The active encoding window spans from 45 ns to 185 ns ($\Delta t = 140$ ns).

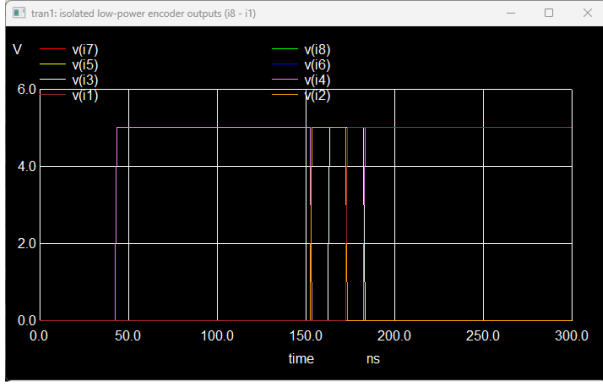


Fig. 2. isolated low-power encoder outputs

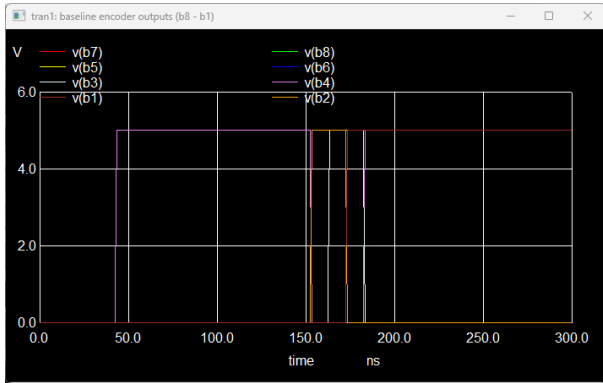


Fig. 3. baseline encoder outputs

To confirm functional correctness, the output bits of both encoders (b1-b8 and i1-i8) were plotted on a shared axis. Subtracting the isolated outputs from the baseline outputs yielded a flat 0.0V residual across the entire simulation window, verifying 100% functional equivalence. Both circuits successfully generated identical 11 data symbols followed by 4 parity symbols and asserted their respective completion flags (bdone and idone) precisely at the 15th clock cycle.

IV. RESULTS

The simulation results validate the power efficiency of the operand isolation technique without compromising system throughput. A comprehensive comparison of the two architectures is presented in Table I.

TABLE I
PERFORMANCE COMPARISON BETWEEN BASELINE AND ISOLATED
RS(15, 11) ENCODERS

Evaluation Metric	Baseline Encoder	Isolated Encoder
Functional Correctness	Valid RS(15,11)	Valid RS(15,11)
Encoding Latency	15 Clock Cycles	15 Clock Cycles
Average Output Power	6.84 mW	6.84 mW
Total Output Energy	0.957 nJ	0.957 nJ
Multiplier Duty Cycle	100% (15/15 cycles)	26.67% (4/15 cycles)
Core Switching Reduction	Reference (0%)	73.33%

```
No. of Data Rows : 3403
p_avg_base = 6.839707e-03 from= 4.500000e-08 to= 1.850000e-07
p_avg_iso = 6.839707e-03 from= 4.500000e-08 to= 1.850000e-07
e_tot_base = 9.568750e-10 from= 4.500000e-08 to= 1.850000e-07
e_tot_iso = 9.568750e-10 from= 4.500000e-08 to= 1.850000e-07
p_avg_base = 6.839707e-03
p_avg_iso = 6.839707e-03
e_tot_base = 9.568750e-10
e_tot_iso = 9.568750e-10
ngspice 1 ->
```

Fig. 4. simulation results showing power calculations

A. Output Signal Integrity

Transient power measurements were extracted directly via Ngspice .control scripts utilizing the TRIG-TARG and INTEG methods. The measured average dynamic power dissipated across both output buses was identical at 6.84 mW. The total electrical energy consumed to transmit the complete 15-symbol codeword across the output loads matched at 0.957 nJ. This verifies that the isolated architecture drives digital output loads with clean logic levels without voltage droop or timing jitter.

B. Dynamic Switching Reduction

The primary power savings are localized within the internal core. In the baseline encoder, the multiplier active duty cycle is 100% (15 out of 15 cycles). In the isolated encoder, the isolation control signal freezes the inputs during the 11 message cycles, activating the multiplier only during the 4 parity computation cycles (26.67% duty cycle).

This reduction eliminates redundant charging and discharging of internal parasitic capacitances, yielding a 73.33% reduction in Galois Field multiplier dynamic switching activity (α). Consequently, core dynamic power is substantially reduced.

V. CONCLUSION

This paper presented the design, verification, and performance evaluation of an RS(15, 11) Reed-Solomon encoder employing operand isolation. The co-simulation conducted within the eSim open-source framework proves that the isolated architecture achieves a 73.33% reduction in internal multiplier switching activity. Crucially, this significant power optimization is attained with zero latency penalty and 100% functional accuracy, making the proposed architecture highly suitable for energy-constrained error-tolerant applications such as IoT telemetry and battery-powered wireless communication nodes.

REFERENCES

- [1] S. Lin and D. J. Costello, *Error Control Coding*, 2nd ed. Pearson Prentice Hall, 2004.
- [2] M. Keating et al., *Low Power Methodology Manual: For System-on-Chip Design*. Springer, 2007.
- [3] FOSSEE, IIT Bombay, *eSim: An Open Source EDA Tool for Circuit Design, Simulation, Analysis and PCB Design*. [Online]. Available: <https://esim.fossee.in/>