

Memristor Emulator with Off-the-Shelf Solid-State Components

eSim Reproduction & Validation Report
Research Migration Project | FOSSEE, IIT Bombay

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Tool chain	eSim 2.5 , Ngspice 35	Source	Yang, Cho, Sah, Kim, Jung — IEEE Conference Publication
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Theory and Description

A memristor is the fourth fundamental passive circuit element, whose resistance (memristance) depends on the history of the charge that has flowed through it, rather than being fixed. Its defining relation is

$$v(t) = R(t) \cdot i(t) = (d\phi/dq) \cdot i(t)$$

where $\phi(t)$ and $q(t)$ are flux and charge. Since ideal memristors are not commercially available, the reference paper reproduces the behaviour of the HP TiO_2 memristor's linear-drift model using an emulator built entirely from off-the-shelf solid-state components (op-amps, resistors, a capacitor, an analog multiplier and MOSFET current mirrors). For the decremental configuration used in this reproduction, the effective input resistance is

$$R_{in} = R_s - (R_T/C) \cdot q_c(t)$$

i.e. the memristance decreases as charge accumulates. The circuit converts the input voltage to a current through an op-amp virtual-ground stage (R_s), integrates that current on a capacitor C to obtain a charge-history voltage, multiplies it with an instantaneous-current voltage (from R_T) using a four-quadrant analog multiplier, and feeds the scaled product back into the input stage, closing the loop that makes R_{in} a function of accumulated charge.

eSim Implementation — Final Verified Component Values

The circuit of Fig. 5 of the reference paper was rebuilt in eSim (KiCad schematic capture with an Ngspice back end) using discrete NMOS/PMOS current mirrors based on $0.5 \mu\text{m}$ technology models, LM741 op-amp macromodels, and two project-specific subcircuits: a four-quadrant behavioural multiplier and a CMOS inverter used to select the current-mirror bias polarity. The parameter set below is the final configuration used for the verified simulations.

Parameter	Value	Parameter	Value
Vdd / Vss	+5 V / -5 V	Rs (R1, input)	16 k Ω
Vin (test signal)	SIN(0, 1, f), 2 Vp-p; f = 100/200/400/800 Hz	Integrator C1	0.5 μF

Parameter	Value	Parameter	Value
Current-mirror technology	0.5 μm (mos_n / mos_p)	Transistor sizing (all mirrors)	$W = 100\text{ }\mu\text{m}$, $L = 100\text{ }\mu\text{m}$
Bias reference R7	20 k Ω	RT branch R11	40 k Ω
Feedback network R2–R10	10 k Ω (uniform)	Multiplier scale factor	1/10 (AD633-style)
Bias-selector state	X5 IN = Vdd; MP4 G/S/B = Vdd	DC-stabilisation	5 M Ω bleeder across C1 + .ic v(C1)=0

The final values were established through node-level operating-point checks, verification of positive/negative current-mirror symmetry, and transient comparison against the expected pinched hysteresis signature. The exact model files used for the verified run are bundled with the project and should be kept unchanged for reproducibility.

Circuit Schematic

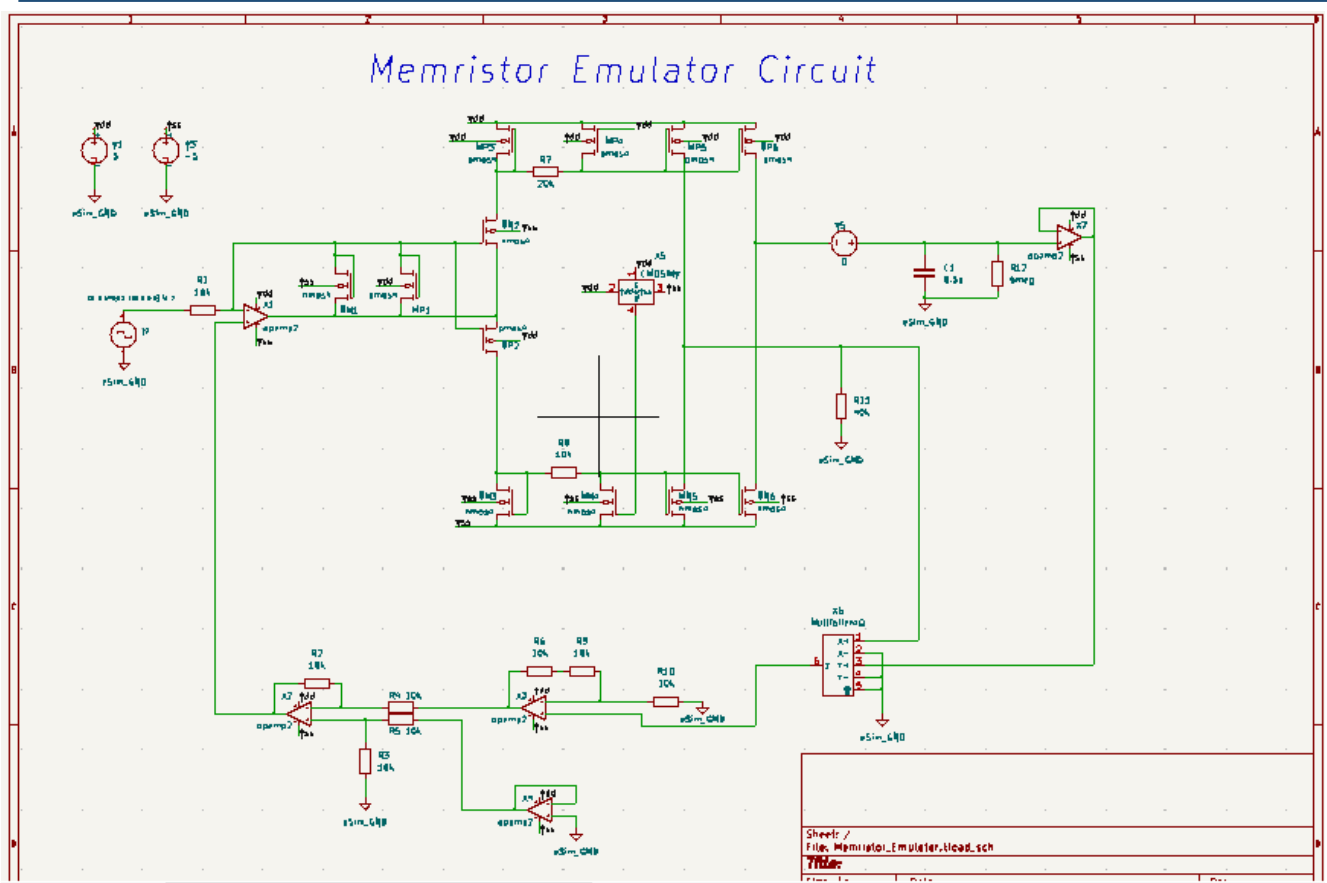


Figure 1. Final eSim/KiCad schematic of the decremental memristor emulator (current-mirror network, custom multiplier subcircuit MU1, feedback amplifier stage, and CMOS inverter X1 for bias polarity selection).

Results: Pinched Hysteresis Loop and Frequency Dependence

The defining signature of memristive behaviour—a pinched hysteresis loop in the input voltage/current plane—was verified for a 2 Vp-p sinusoidal input at 100, 200, 400 and 800 Hz, reproducing the qualitative test of Fig. 6 and Fig. 7 in the reference paper. The 100 Hz loop is clearly open and pinched at the origin; as frequency increases, the loop narrows because less charge history accumulates during each cycle.

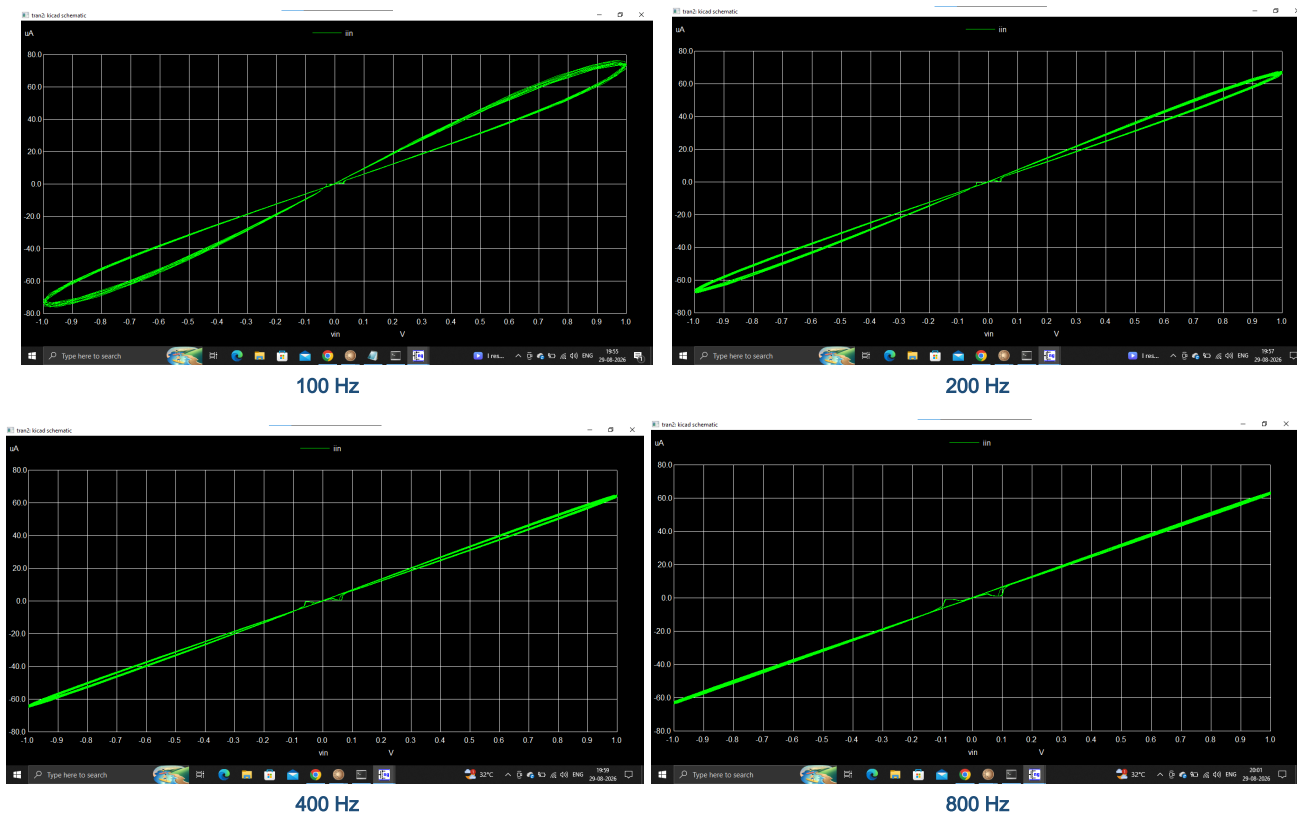


Figure 2. Simulated i_{in} vs. v_{in} pinched hysteresis loops at four test frequencies, reproducing the qualitative trend of the reference paper (loop area decreases monotonically with increasing frequency)

Quantitative Comparison with the Reference Paper

Quantity	Published value (paper)	eSim result	Comparison
Loop shape @ 100 Hz	Pinched hysteresis, passes through origin (Fig. 6)	Two-lobed pinched hysteresis observed; origin crossing reproduced	Qualitative match confirmed
Loop trend, 100–800 Hz	Loop area narrows with increasing frequency	Loop area narrows with increasing frequency	Trend matches
Input signal	100/200/400/800 Hz, 2 Vp-p sinusoid	Same: $\text{SIN}(0, 1, f)$, $f = 100/200/400/800$ Hz	Exact match
Supply	± 5 V	± 5 V	Exact match
R_s (decremental)	~ 16 k Ω	16 k Ω	Exact match
Peak i_{in} @ 100 Hz	Not tabulated numerically	≈ 76 μA	Not numerically tabulated in paper
Memristance range	~ 0 –19 k Ω (Fig. 8, slope estimate)	Not extracted numerically	Not compared
Non-volatility	Memristance holds during idle interval	Residual leakage ≈ 49 nA	Near-hold; finite bleeder leakage

Design Validation Summary

The final configuration was reached by resolving a small set of implementation and model-interface issues that materially affected current-mirror symmetry, integrator stability, and XY plotting. The points below are important for reproducing the verified result.

- All MOSFETs use explicit bulk/substrate connections (NMOS → Vss, PMOS → Vdd) and explicit sizing $W = 100\text{ }\mu\text{m}$, $L = 100\text{ }\mu\text{m}$, $M = 1$.
- The LM741 project copy must use the verified external pin declaration “.subckt lm741 1 2 99 50 28”. An incorrect input-pin mapping drove the front-end stage into saturation and destroyed the bidirectional current conversion.
- The verified PMOS technology-library copy uses $V_{MAX} = 1.0E05$. The stock $V_{MAX} = 0.3u$ value suppressed PMOS mirror current to the nA range and prevented symmetric positive/negative operation; therefore the exact project-local model file must be distributed with the schematic.
- The working decremental bias-selector state is X5 input tied to Vdd, with MP4 gate/source/bulk tied to Vdd. The CMOS inverter output consequently drives the MN4 selector gate low.
- A 5 M Ω bleeder across C1 together with “.ic v(C1)=0” provides a well-defined startup condition for the current-fed integrator without materially altering the short-timescale hysteresis test.
- Ngspice XY plotting must use the “retraceplot” option. A plain “plot iin vs vin” suppresses the retracing part of the non-monotonic X trajectory and can make a valid hysteresis loop appear as a single curve.

Reproducibility — Running this Project in eSim

1. Open eSim → Open Project and load the project directory containing the .kicad_sch file.
2. Keep the exact verified model files with the project: lm741.sub, CMOSInverter.sub, Multiplier4Q.sub, NMOS-0.5um.lib and PMOS-0.5um.lib. If the project is moved, re-link these files before netlist conversion. Verify “.subckt lm741 1 2 99 50 28” and PMOS “ $V_{MAX}=1.0E05$ ”.
3. Open the schematic and verify the final component values. Critical wiring checks are X5 IN → Vdd, MP4 G/S/B → Vdd, NMOS bulks → Vss, PMOS bulks → Vdd, and $W=100u$ $L=100u$ $M=1$ on every MOSFET.
4. Generate the KiCad netlist and run Convert KiCad to Ngspice. Do not manually repair topology after conversion; a fresh conversion should already reproduce the verified connections.
5. For the 100 Hz reference run, use $V_{in} = \text{SIN}(0\ 1\ 100\ 0\ 0\ 0)$, $C1 = 0.5u$, and a settled-cycle transient window: “.tran 1u 50m 40m 1u” with “.ic v(net-_c1-pad1_)=0”.
6. Run the simulation and plot the input current against the input voltage with the Ngspice retracing option. The exact control block used for the verified plot is shown below.

```
.control
run

let vin = v("net-_r1-pad1_")
let iin = -i(v2)

plot iin vs vin retraceplot

.endc
```

7. For the frequency comparison, change only the V_{in} frequency to 200, 400 and 800 Hz. For a single settled cycle ending at 50 ms, useful display windows are 45–50 ms (200 Hz), 47.5–50 ms (400 Hz), and 48.75–50 ms (800 Hz).
8. For state-variable verification, plot $v(\text{net_c1-pad1_})$ versus time. The 100 Hz result should show a two-lobed pinched iin–vin loop; increasing frequency should progressively narrow the loop.

Project Directory Contents

File / item	Purpose
*.kicad_sch, *.kicad_pro	Main schematic and project files
*.cir, *.cir.out	Generated and Ngspice-ready netlists / simulation outputs
lm741.sub	Project-local LM741 macromodel; verified external pin declaration: 1 2 99 50 28
Multiplier4Q.sub	Custom four-quadrant multiplier implemented with an Ngspice behavioural B-source
CMOSInverter.sub	Custom CMOS inverter used for the verified bias-polarity selector state
NMOS-0.5um.lib / PMOS-0.5um.lib	Verified 0.5 μm technology models; bundled PMOS copy uses VMAX=1.0E05

Limitations

- The 5 M Ω bleeder used to establish the integrator DC operating point introduces a small finite leakage that is absent from the ideal mathematical model.
- The feedback amplifier network R2–R10 is kept at a uniform nominal 10 k Ω and was not independently optimized against the exact closed-loop scaling of the reference derivation; additional tuning could improve quantitative agreement.
- The four-quadrant multiplier is implemented as an idealized Ngspice behavioural B-source rather than a transistor-level Gilbert-cell multiplier or a specific hardware multiplier macromodel.
- The exact min/max memristance and loop area have not been extracted numerically in this report; the validation is therefore primarily qualitative, based on the pinched-loop shape and its frequency narrowing.
- Reproducibility depends on using the bundled, verified model files—especially the project PMOS technology file and the verified LM741 pin mapping—rather than unmodified library copies from another installation.

Conclusion

The decremental memristor emulator of Yang et al. was reproduced in eSim using discrete 0.5 μm NMOS/PMOS current mirrors, LM741 op-amp macromodels, a behavioural four-quadrant multiplier, and a CMOS bias-polarity inverter. After correcting the model interface, bias-selector state, integrator startup, and Ngspice XY retracing, the circuit reproduces the central memristive signature: a two-lobed pinched hysteresis loop in the v_{in} – i_{in} plane that narrows as the input frequency increases. The result is qualitatively consistent with the reference design, while quantitative extraction of the full memristance range and further feedback-network optimization remain suitable follow-up work.

Reference

C. Yang, S. Cho, M. P. Sah, H. Kim, and K.-S. Jung, "Memristor Emulator with Off-the-shelf Solid State Components for Memristor Application Circuits," IEEE. <https://doi.org/10.1109/CNNA.2012.6331432>