

Abstract

This work presents the reproduction and simulation of a **Hybrid Clock and Data Gating for Low-Power RV32I Processor**, a digital IP designed to reduce unnecessary switching activity and dynamic power consumption in a 32-bit RISC-V architecture. The processor follows a five-stage pipeline comprising Instruction Fetch, Instruction Decode, Execute, Memory Access, and Write-Back stages. A Hybrid Gating Network and Hybrid Gating Controller are incorporated to selectively control clock activity in sequential modules and suppress redundant data transitions in combinational and memory-related modules. Clock gating is applied to the Program Counter, pipeline registers, and Register File, while data gating is used for modules such as the ALU input path and Data Memory interface. The gating operation is controlled according to instruction type, control signals, and pipeline activity. The design is reproduced as a digital IP and verified through simulation by observing input-output and enable-control waveforms during arithmetic, memory, active, and idle operations. The expected outcome is correct RV32I processor functionality with reduced unnecessary switching activity, demonstrating an effective low-power design methodology suitable for FPGA-based and energy-efficient digital systems.