



Research Migration Project

<https://esim.fossee.in/research-migration-project>



The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit : Hybrid Clock and Data Gating for Low-Power RV32I Processor

Theory/Description : The proposed work presents a 32-bit RV32I RISC-V processor designed using a hybrid clock and data gating methodology to reduce unnecessary switching activity and dynamic power consumption. The processor follows a conventional five-stage pipeline architecture consisting of Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Memory Access (MEM), and Write-Back (WB) stages. A Hybrid Gating Network (HGN) and Hybrid Gating Controller (HGC) monitor processor activity and control the operation of the functional modules based on instruction requirements and pipeline activity.

Clock gating is applied to sequential modules such as the Program Counter, pipeline registers, and Register File. When a pipeline stage is idle or executing a NOP instruction, the corresponding clock-enable signal disables unnecessary clock transitions. Data gating is applied to combinational and data-processing blocks such as the ALU and Data Memory interface, where operand or data transitions are suppressed when the corresponding operation is not required. The Hybrid Gating Controller uses control signals including RegWrite, MemRead, and MemWrite to generate clock-enable and data-gating enable signals.

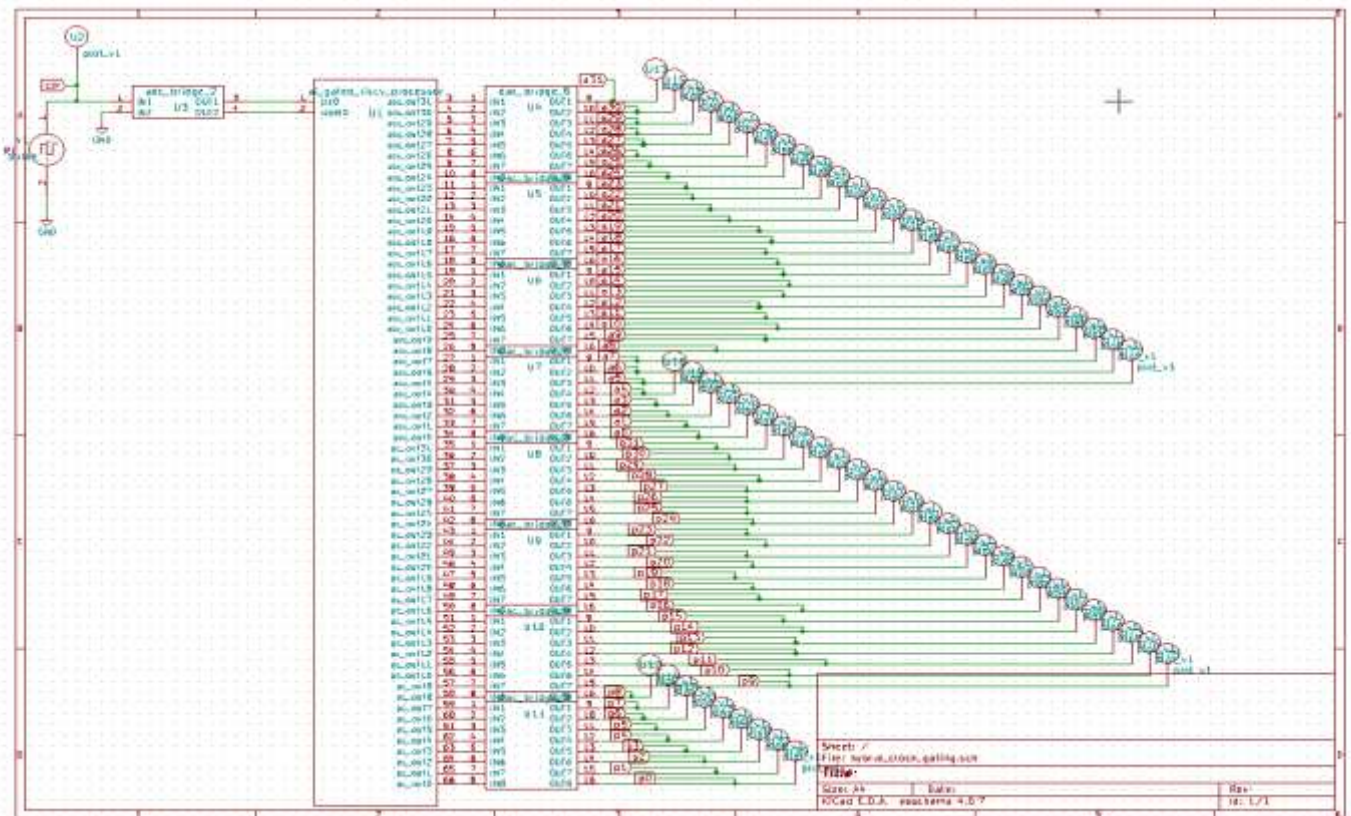
Reason to reproduce with eSim : This design is suitable for reproduction and analysis using eSim because it demonstrates important low-power VLSI design concepts at the digital and circuit-design level. The hybrid gating methodology can be studied by implementing and analyzing the clock-enable and data-enable logic used to control unnecessary switching activity. Using eSim with Ngspice, the gating circuits can be examined to observe signal transitions, enable-controlled operation, and the effect of reducing redundant switching on power consumption.

The simulation platform also provides waveform visualization for verifying the gating behavior during active and idle conditions. Individual logic blocks associated with clock and data gating can be reproduced and analyzed to understand how enable signals selectively control circuit activity. This makes the work suitable for academic learning and research-oriented experimentation in low-power digital VLSI design. The paper itself validates the proposed architecture through functional simulation and power analysis based on switching activity.

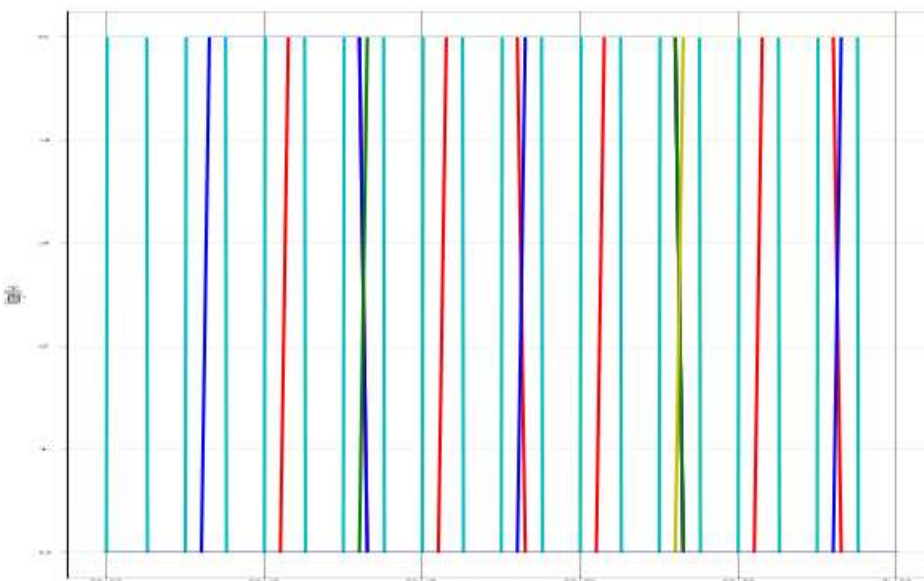
Expected Outcome/outputs: The reproduced design is expected to demonstrate correct gating behavior, where clock and data transitions are enabled only when the corresponding processor modules are required for instruction execution. During idle cycles, NOP conditions, or instructions that do not require specific functional units, unnecessary switching activity will be suppressed.

The expected results include proper enable-controlled waveforms, reduced redundant signal transitions, and correct functional operation during arithmetic and memory-related instructions. According to the paper's FPGA power analysis, the hybrid-gated design reduced total power consumption from **0.187 W to 0.135 W**, corresponding to a **27.8% reduction**, while dynamic power decreased from **0.094 W to 0.044 W**, giving a **53.2% reduction**. The design also showed negligible resource overhead, using 85 LUTs and 31 flip-flops in the reported post-synthesis implementation. Therefore, the expected outcome is a functionally correct low-power RV32I processor architecture with significantly reduced switching and dynamic power consumption.

Schematic Diagram :



Simulation Output:



Block Diagram (s) :

Single top-level block showing:

Inputs: Clock (CLK), Reset, Instruction/Data inputs, and processor control signals.

Processing Block: 32-bit five-stage RV32I processor incorporating the **Hybrid Gating Controller (HGC)** and **Hybrid Gating Network (HGN)**. The controller monitors pipeline activity and control signals and selectively enables or disables clock and data activity in the processor modules.

Gated Modules: Program Counter, Pipeline Registers, Register File, ALU Input Buffers, Data Memory Interface, and Write-Back path.

Outputs: Processed instruction results, write-back data, processor output signals, and gating enable signals.

Expected Results (Input, Output waveforms and/or Multimeter readings) :

The expected output will be obtained through **digital RTL simulation waveforms** rather than multimeter readings. The simulation should verify correct execution of RV32I instructions such as **ADD, SUB, LW, and SW**, along with the operation of the hybrid clock and data gating mechanism.

Expected waveforms will show:

Correct clock and reset operation.

Proper instruction execution through the **IF, ID, EX, MEM, and WB** pipeline stages.

CLK_EN = 1 when a sequential module or pipeline stage is active and **CLK_EN = 0** during idle or NOP conditions, preventing unnecessary clock transitions.

DG_EN = 1 when valid ALU or memory data processing is required and **DG_EN = 0** when unnecessary data transitions must be suppressed.

ALU and Data Memory-related signals remaining inactive or masked when the corresponding instruction does not require those modules.

Correct write-back operation to the Register File.

Functional correctness during both active and idle processor cycles without timing or functional errors.

The reported implementation results show that the hybrid-gated processor achieved a reduction in total power from **0.187 W to 0.135 W (27.8%)** and dynamic power from **0.094 W to 0.044 W (53.2%)**, demonstrating the effectiveness of reducing unnecessary switching activity.

Research Paper/Journal/etc. :

- **Title:** "Hybrid Clock and Data Gating for Low-Power RV32I Processor on FPGA"
- **Author:** S.Rosaline, Beer Mohammed Irfan Z , JugeshSai N , Praveen Kumaar V , Harjith R, Bhavithravan C A.
- **Link:** <https://ieeexplore.ieee.org/document/11620201>

Source/Reference(s) :

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Varasala, P., Karapa, B., and Maddu, K. "Intelligent Clock Gating for FPGA-based RISC Architectures: A Novel Approach to Switching Activity and Dynamic Power Reduction," *International Journal of Computer (IJC)*, 2024.

Sathish, S., Prajwal, P. N., Akshaya, A. R., Kastubha, K., and Kumar, S. "Impact of Clock-Gating on ALU Optimized RISC-V Microarchitectures for Low Power Applications," 2025.

eSim Documentation: [eSim FOSSEE Resources](#)