

TITLE: Low Power Design and Simulation of MGDI-Based Circuits: 8T Full Adder and D-Latch Using eSim

STUDENT NAME: BEJISH S

MENTOR NAME: DR. R.M. BOMMI

COLLEGE: CHENNAI INSTITUTE OF TECHNOLOGY

PROBLEM STATEMENT:

Develop and Simulate low power and high efficient 8T Full Adder and D-Latch using the Modified Gate Diffusion Input (MGDI) technique to reduce the circuit complexity by reducing the number of transistors used and to enhance the performance of the circuit by reducing the power consumption and time delay.

ABSTRACT:

The 8T Full Adder and D-Latch were designed using MGDI logic that is an efficient low-power technique for digital circuits. The 8T Full Adder contains a set of gates designed for binary addition. In this design, the logic was optimized in order to consume less power at high speed of operation, thus using 8 transistors for the entire circuit. This MGDI-based logic gate helps in the realization of carry and sum generation without power dissipation, which can be lessened compared to CMOS designs. Similarly, for storing a bit of data in a sequential circuit, the D-Latch is made from MGDI logic gates to ensure that it operates on low power with minimal delay. In both circuits, the design at the transistor level is done by using PMOS and NMOS transistors to ensure a high performance rate and low power consumption.

APPLICATIONS:

The 8T Full Adder is mainly applied in arithmetic and logic units (ALUs) to perform addition in digital systems. It is low power and high speed, thus suitable for use in energy-constrained devices, such as mobile phones, embedded systems, and portable electronics. The D-Latch is applied in sequential circuits for data storage and timing control. It is used for registers, memory units, and flip-flops where low-power consumption is imperative to maintain a system's performance in energy efficient designs. Designed with MGDI logic and then simulated in eSim, the two circuits propel the development in low-power digital circuit design having high performance.

CIRCUIT DIAGRAMS:

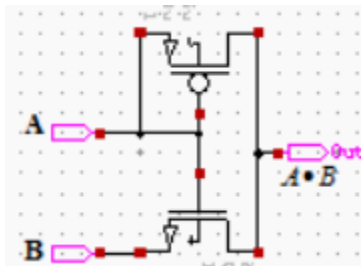


Fig 1: AND Gate

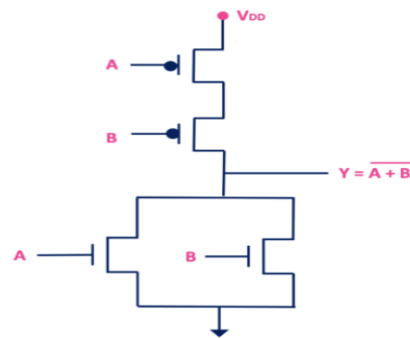


Fig 2: NOR Gate

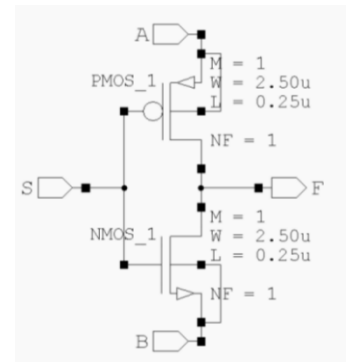


Fig 3: 2x1 MUX

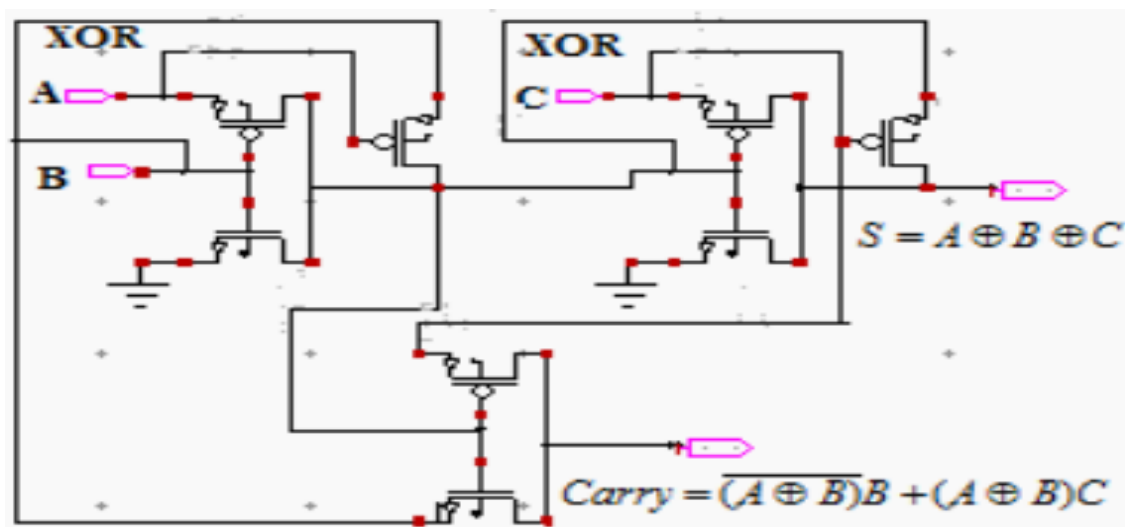


Fig 4: 8T Full Adder using MGD1 Technique

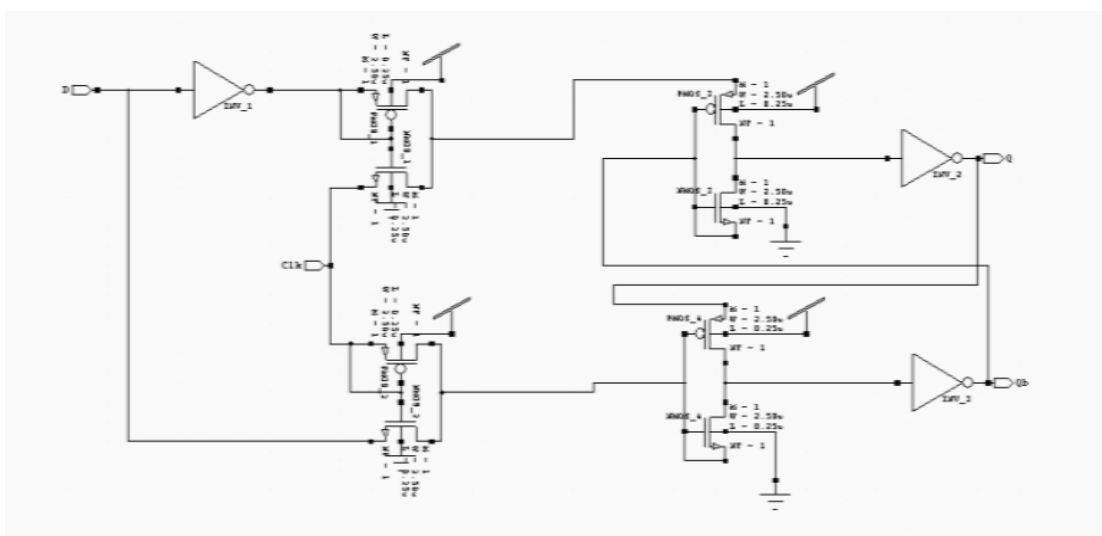
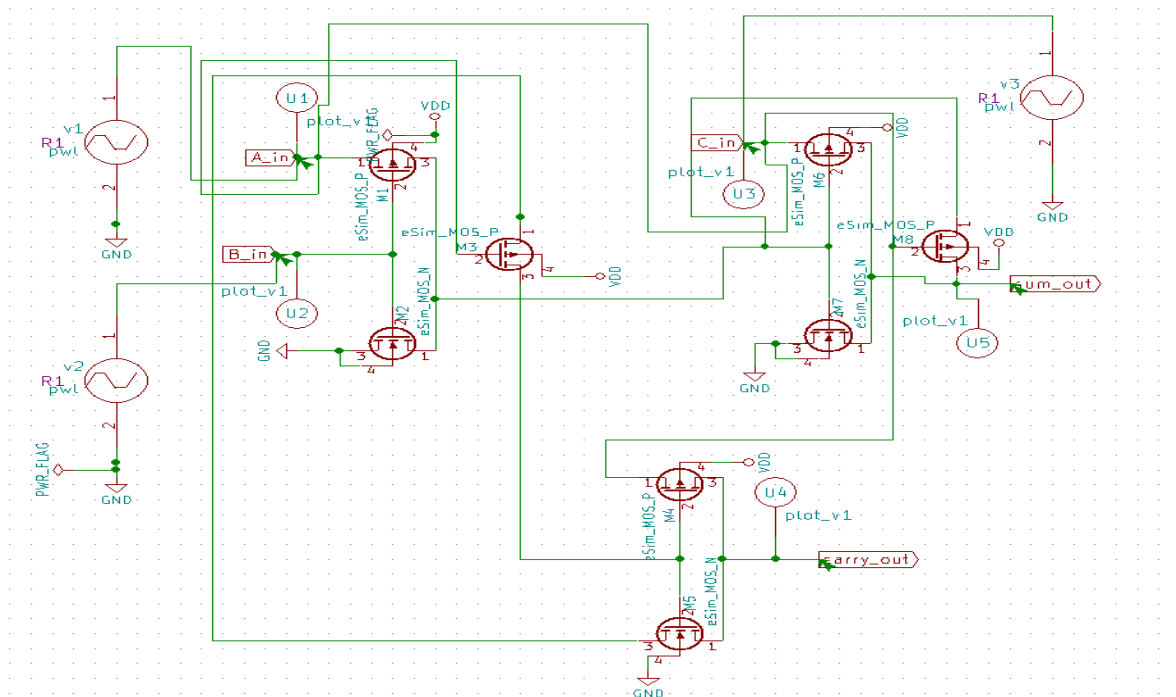
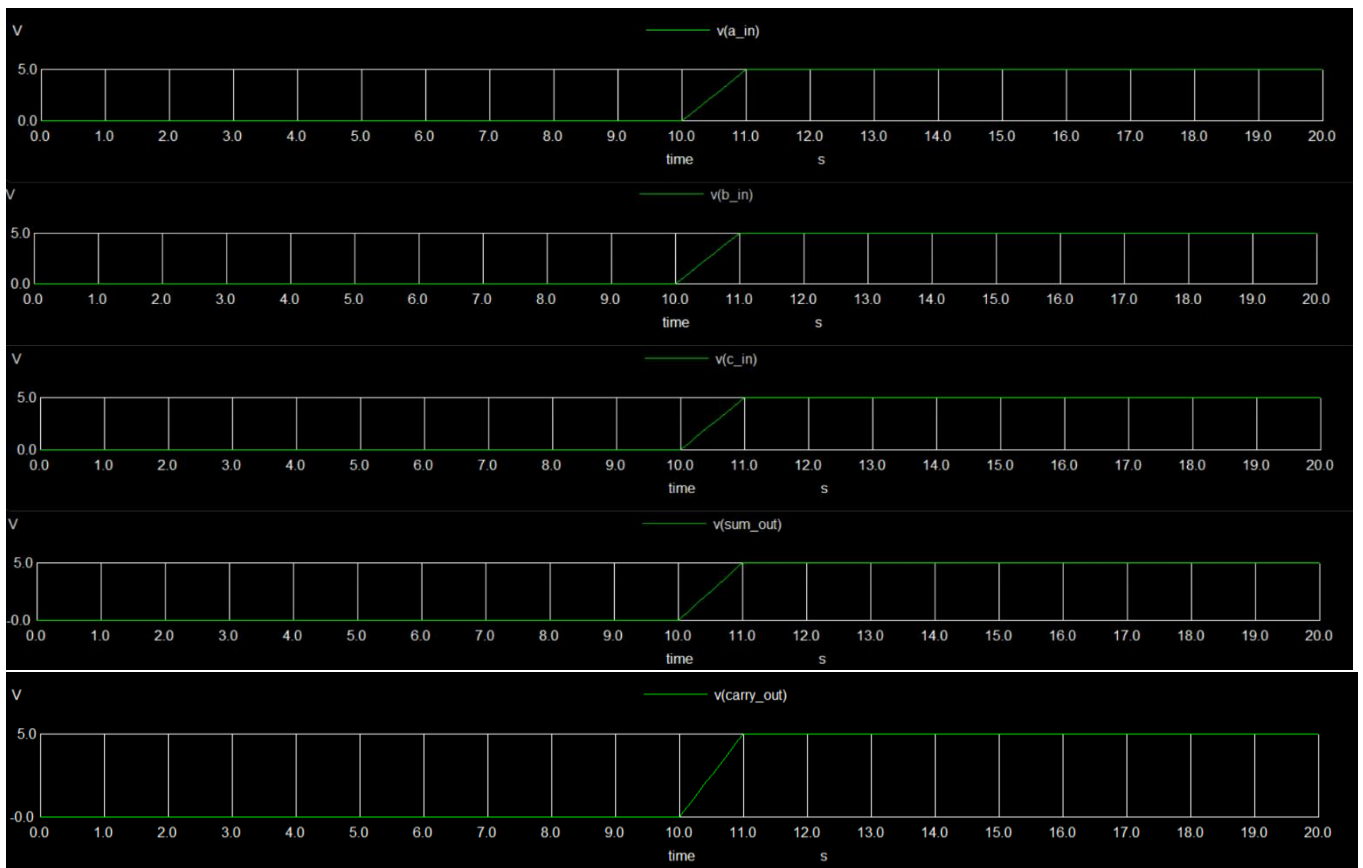


Fig 5: D-Latch using MGD1 Technique

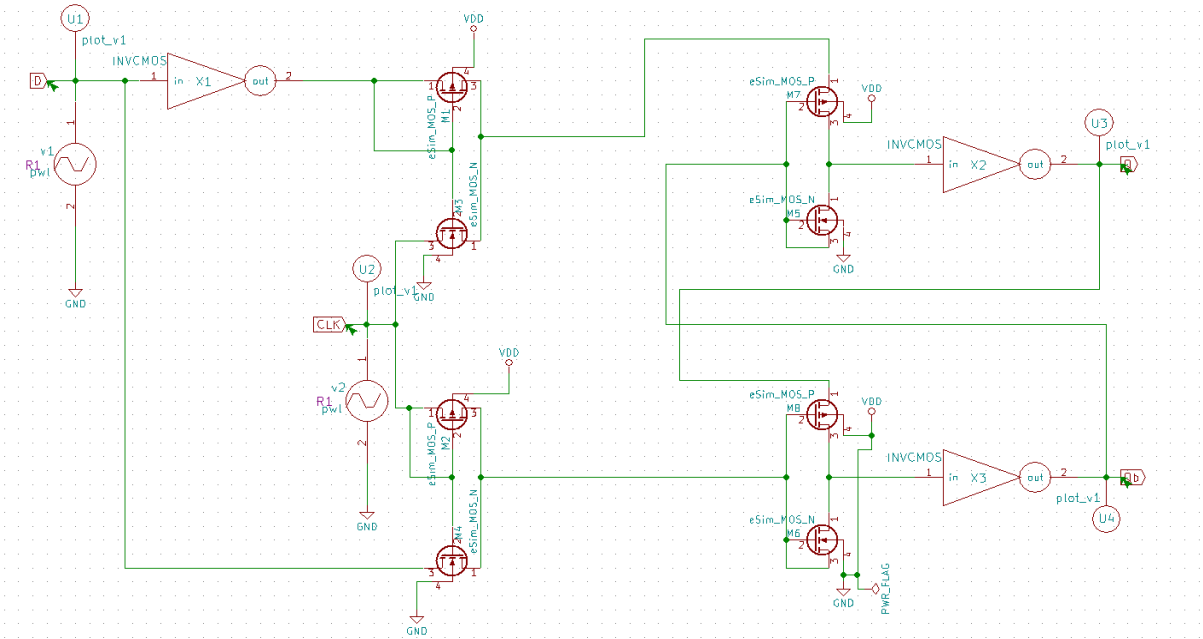
CIRCUIT DIAGRAM OF 8T FULL ADDER USING MGDI IN eSim:



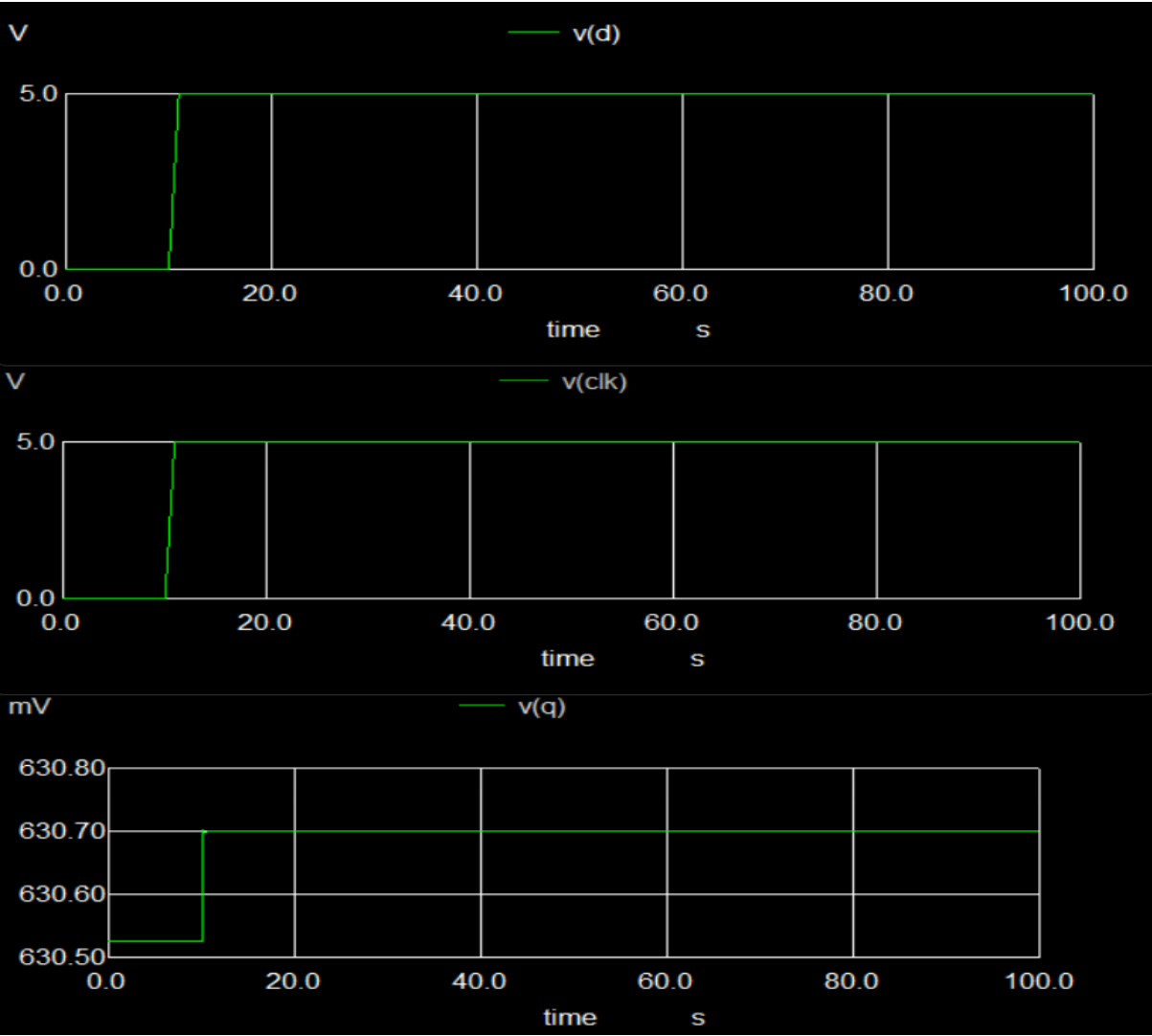
OUTPUT OF 8T FULL ADDER USING eSim:



CIRCUIT DIAGRAM OF D-LATCH USING MGD1 IN eSim:



OUTPUT OF D-LATCH USING eSim:



REFERENCES:

- [1] R. Uma and P. Dhavachelvan, “Modified Gate Diffusion Input Technique: A New Technique for Enhancing Performance in Full Adder Circuits,” *Procedia Technology*, vol. 6, pp. 74–81, 2012, doi: 10.1016/j.protcy.2012.10.010.
- [2] S. Savadipalayam Venkatachalam Principal, A. Professor, and S. Sivasubramaniyam Professor, “Design of Low Power Flip Flop Based on Modified GDI Primitive Cells and Its Implementation in Sequential Circuits Design of Low Power Flip Flop Based on Modified GDI Primitive Cells and Its Implementation in Sequential Circuits Sivakumar Sabapathy Arumugam,” 2017. [Online]. Available: www.ijaceeonline.com