

# Research Migration Project

<https://esim.fossee.in/research-migration-project>



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The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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**Title of the circuit :** Design and Simulation of a conventional 1T1C DRAM Sensing Circuit and a Redundant Voltage Discharged Single Bitline Load Sense Amplifier (RVD-SBLSA)

**Theory/Description :** A 1T1C DRAM cell stores a single bit using the charge stored in a capacitor, called the storage capacitor ( $C_s$ ). An NMOS transistor is used to connect the cell to the bitline. The gate of this transistor is connected to the wordline (WL), so the cell can be accessed when WL is turned ON.

The voltage change produced on the bitline during a read is very small because the storage capacitor is much smaller than the capacitance of the bitline. Therefore, this small voltage difference cannot be used directly as a logic 0 or 1. A sense amplifier is used to detect this difference and convert it into a full logic level.

Before reading the cell, BL and BLB are first precharged to around  $(V_{DD})/2$ . When WL is enabled, the charge stored in the cell capacitor is shared with the bitline. Depending on whether the cell stores 0 or 1, a small voltage difference appears between BL and BLB. The cross-coupled inverters in the sense amplifier then amplify this small difference. As sensing continues, one bitline moves towards  $(V_{DD})$  while the other moves towards 0 V. The sensing operation also restores the data in the cell, since a DRAM read is destructive.

The RVD-SBLSA used in this work is a modified version of the conventional sense amplifier. The main difference is the addition of the N4/P4 and N5/P5 transistor pairs, which help separate the reference bitline from the main sensing circuit during part of the operation. It also uses two diode-connected NMOS transistors, N6 and N7, to control the bitline voltage during the discharge stage.

The main idea behind this modification is to avoid unnecessarily charging the reference bitline up to  $(V_{DD})$  and then bringing it back to  $(V_{DD})/2$  after sensing. This repeated voltage swing consumes extra energy. By controlling the bitline discharge differently, the proposed circuit aims to reduce the energy required for each DRAM read operation while still performing the sensing and restoration correctly.

## Circuit Diagram(s) :

The circuits shown below are the ones implemented and simulated in eSim for this project.

Fig. A represents the conventional 1T1C DRAM cell along with the precharge circuit and the cross-coupled CMOS sense amplifier. The schematic also includes the control signals such as SAP, SAN, ENABLE and ENABLEBAR, along with CSEL and the write-driver section. The required DC and transient sources have also been added to provide the supply voltages and timing signals during simulation.

Fig. B shows the RVD-SBLSA circuit used for comparison with the conventional design. In addition to the main sense-amplifier circuit, this schematic contains the extra N4/P4 and N5/P5 transistor pairs used for isolation. The N6 and N7 transistors are diode-connected and are used during the discharge part of the operation. The control signals DCG, LRA and NLRA are provided through the corresponding sources in order to test the discharge operation of the proposed circuit. Both schematics were set up in eSim so that their transient behaviour could be observed and compared under the required DRAM read and write conditions.

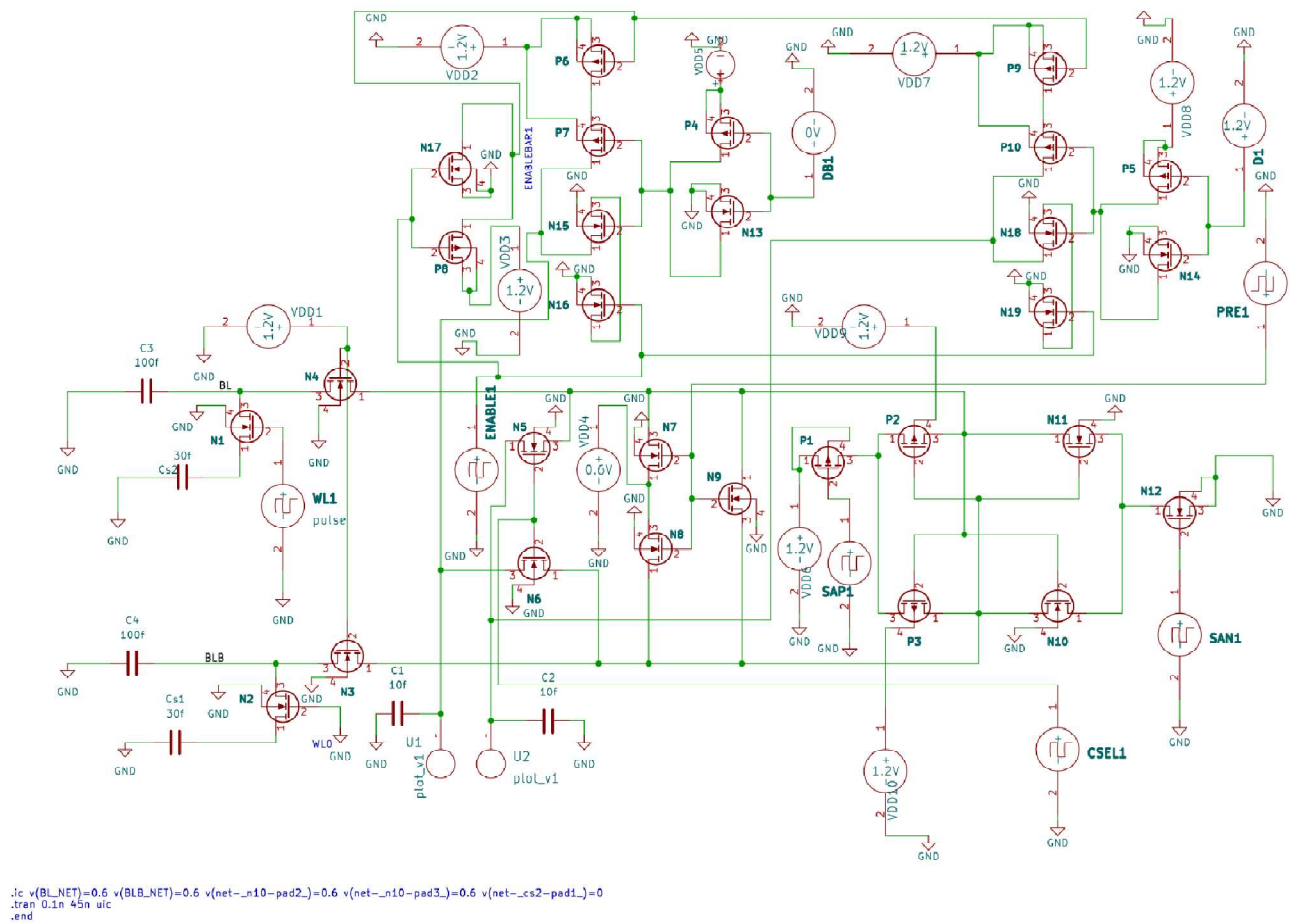


Fig. A: eSim schematic of the conventional 1T1C DRAM sensing circuit

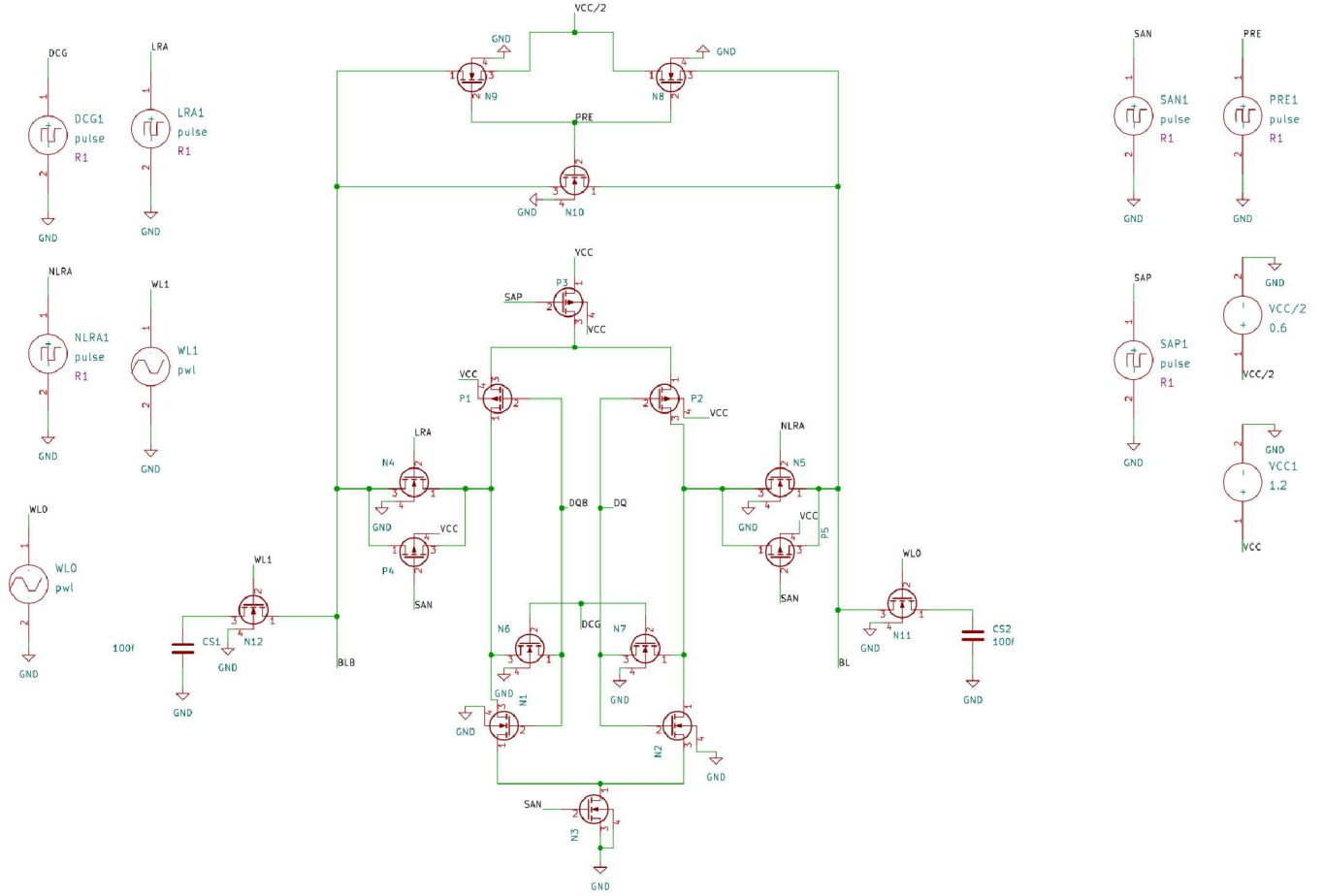


Fig. B: eSim schematic of the RVD-SBLSA circuit.

### Simulation Setup:

Both circuits were built and simulated in eSim (Kicad & ngspice) using standard NMOS/PMOS device models available in the open-source design kit, in place of the proprietary 65 nm technology used in the original publication. Each circuit was exercised through the precharge → sensing → post-sense (I/O) sequence for the four DRAM operations of interest. Transient analysis was used to obtain the BL (red trace) and BLB (blue trace) voltage waveforms shown below; the x-axis is time (seconds) and the y-axis is voltage (V).

For circuit 1, different voltages were given to DB and D for the 4 different conditions:

| CONDITION          | V_(DB) | V_(D) | V_Cs2 |
|--------------------|--------|-------|-------|
| Read '0'           | 1.2    | 0     | 0     |
| Read '1'           | 0      | 1.2   | 1.2   |
| Read '0' Write '1' | 0      | 1.2   | 0     |

|                    |     |   |     |
|--------------------|-----|---|-----|
| Read '1' Write '0' | 1.2 | 0 | 1.2 |
|--------------------|-----|---|-----|

The library chosen for both the circuits transistor was 180nm library of eSim. The W/L was changed accordingly in both circuits' device modelling.

Note: because generic ngspice device models were used instead of the 65 nm technology in the reference paper, the absolute voltage levels, timing, and settling behaviour differ somewhat from the published results. The waveforms below are presented as the qualitative validation of circuit operation for this project; some of the operation labels correspond approximately to the cases discussed in the reference paper given the time constraints of this submission.

## Results:

### 1. Conventional 1T1C DRAM Sense Amplifier — BL/BLB Waveforms

Fig. 1 shows the simulated BL and BLB waveforms for the conventional sense amplifier during the four DRAM operations: read '0', read '1', read '0'-write '1', and read '1'-write '0'. The BL waveform is shown in red, while BLB is shown in blue. Initially, both bitlines are kept at about  $(V_{DD}/2)$ , which is around 0.14 V in our simulation. When WL is turned ON, the cell gets connected to the bitline and charge sharing takes place. This causes a small difference between the voltages of BL and BLB. The sense amplifier then detects this small difference and starts driving the two bitlines in opposite directions. One bitline rises while the other falls until they reach their respective logic levels. The four plots show this behaviour for the different read and read-write cases. Thus, the simulation confirms that the conventional sense amplifier is able to distinguish the stored data and produce the required bitline output.

Fig. 1(a): Read '0' operation — BL/BLB sensing waveform

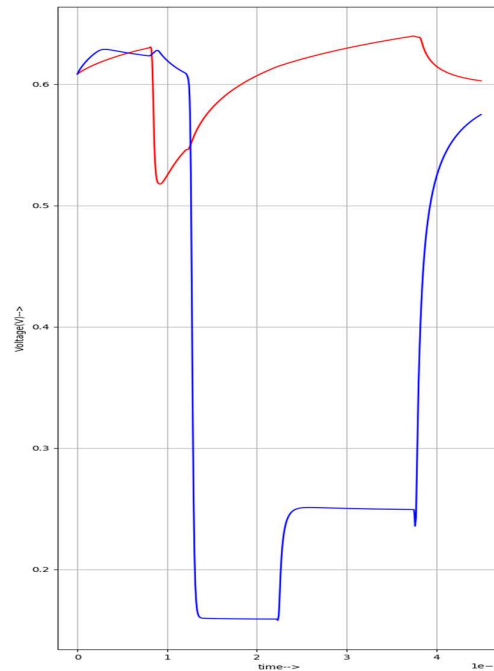


Fig. 1(b): Read '1' operation — BL/BLB sensing waveform

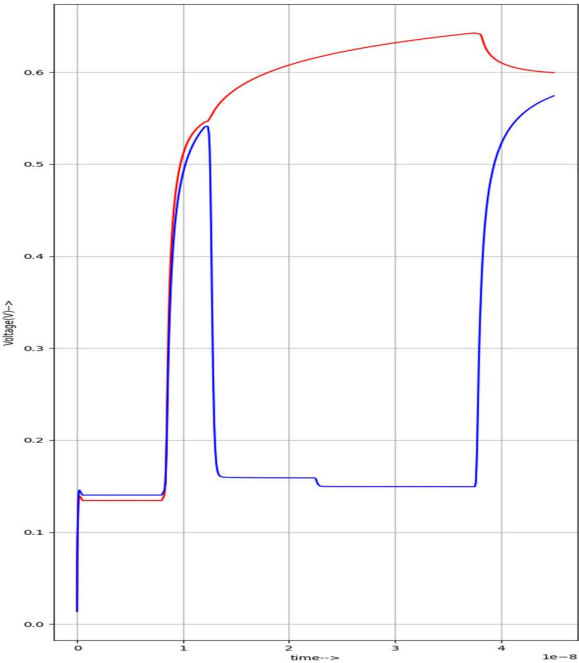


Fig. 1(c): Read '0' – Write '1' operation — BL/BLB sensing and write-back waveform

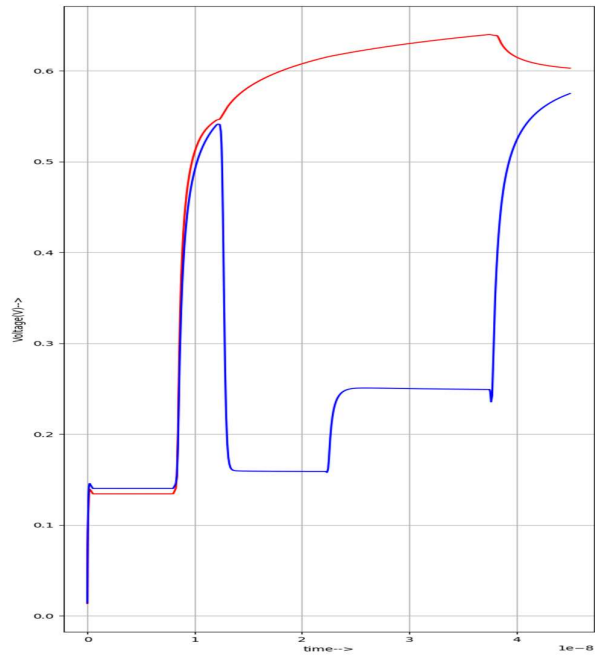
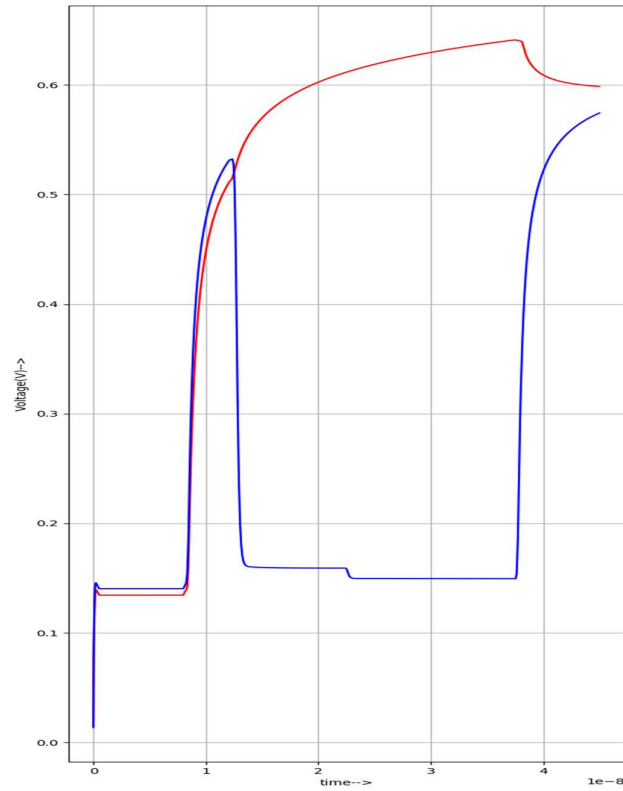


Fig. 1(d): Read '1' – Write '0' operation — BL/BLB sensing and write-back waveform

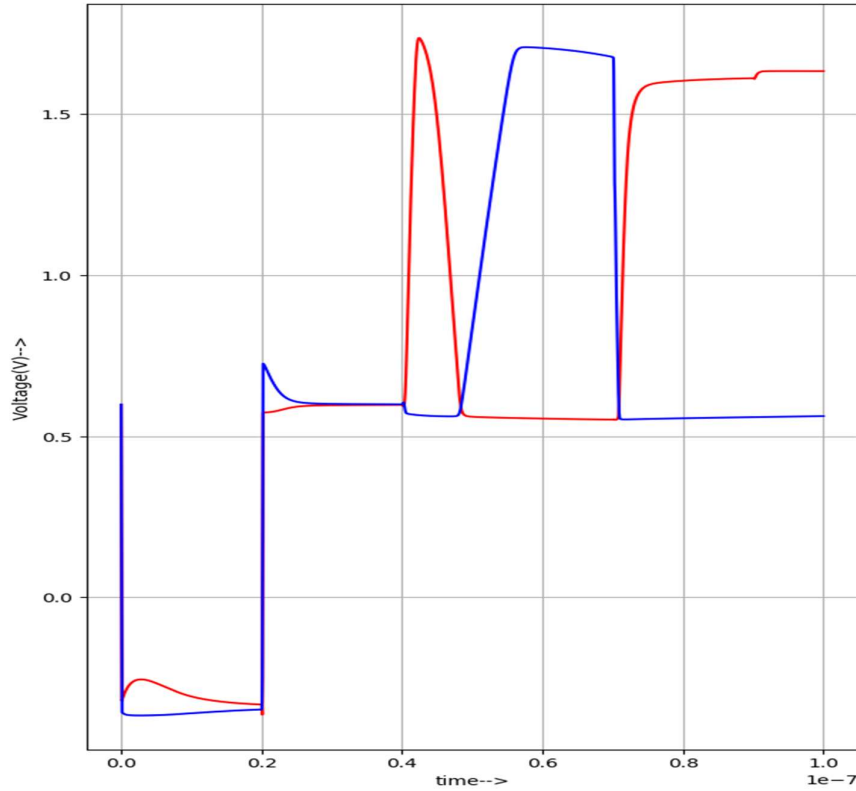


In the read '0' and read '1' cases (Fig. 1a, 1b), the bitline pair separates during the sensing window and settles to a stable low/high pair, consistent with the expected DRAM read behaviour. In the read-write cases (Fig. 1c, 1d), an additional I/O transition is visible after the initial sense phase — the bitline pair steps to a second voltage level once the write driver overrides the sensed data — before the circuit is reset for the next precharge cycle.

## 2. RVD-SBLSA — Extended Sensing/Discharge Behaviour:

Fig. 2 shows the RVD-SBLSA waveforms for two consecutive DRAM access cycles. A longer simulation time is used here so that the complete sequence, including the discharge and recovery period, can be seen clearly. This waveform corresponds to Fig. 6 of the original study.

Fig. 2: RVD-SBLSA extended waveform over two consecutive sensing/discharge cycles (BL – red, BLB – blue).



One noticeable difference from the conventional sense amplifier is what happens to the reference bitline after sensing. Instead of remaining at the high supply level until the next operation, the bitline is brought down towards  $(V_{DD})/2$  during the discharge stage. This is done using the diode-connected NMOS transistors N6 and N7.

After this recovery step, the circuit enters the next precharge cycle. The important point here is that the reference bitline does not have to make the complete transition from  $(V_{DD})$  back to  $(V_{DD})/2$  during every cycle. By reducing this unnecessary voltage swing, the RVD-SBLSA can reduce the energy consumed during repeated DRAM accesses. The waveform therefore helps show the main reason for adding the discharge section to the proposed sense amplifier.

### Discussion:

From the simulations, the main behaviour of the circuits can be seen as expected. In the conventional sense amplifier, the bitlines first start from the precharge level of around  $(V_{DD})/2$ . After the cell is

connected, charge sharing creates a small voltage difference between BL and BLB. The sense amplifier then increases this difference and drives the two bitlines towards their logic levels.

The RVD-SBLSA shows the same basic sensing operation, but an additional discharge step can be seen after sensing. During this part of the cycle, the reference bitline is brought back towards  $(V_{DD})/2$  instead of simply staying at the full supply voltage. This is the main behaviour that I wanted to verify from the proposed circuit.

The simulations were performed using the available generic ngspice MOS models rather than the original 65 nm technology models used in the paper. Because of this, the voltage values and timing of the waveforms are not exactly the same as those reported in the paper. I also did not complete a detailed energy calculation for both circuits within the available project time. Therefore, the results should mainly be considered a functional reproduction of the circuit operation. The important switching, sensing and discharge behaviour was reproduced, but the simulation should not be treated as an exact numerical reproduction of the published results.

### **Conclusion:**

The conventional 1T1C DRAM sense amplifier and the RVD-SBLSA circuit from Dai et al. (2023) were reproduced and simulated in eSim/ngspice. The transient BL/BLB waveforms obtained for the read '0', read '1', read '0'-write '1', and read '1'-write '0' operations, along with the extended RVD-SBLSA discharge/recovery waveform, demonstrate that the basic sensing, amplification, and (for RVD-SBLSA) energy-saving discharge mechanism described in the reference paper can be reproduced using an open-source simulation flow.

Due to time constraints, the figure labelling and the quantitative energy comparison between the two circuits are approximate and are recommended as follow-up work.

### **Research Paper / Journal / Source:**

- Title: Low-Power Single Bitline Load Sense Amplifier for DRAM
- Authors: Chenghu Dai, Yixiao Lu, Wenjuan Lu, Zhiting Lin, Xiulong Wu, Chunyu Peng
- Journal: Electronics, 2023, 12, 4024, Pages 1–12
- DOI: <https://doi.org/10.3390/electronics12194024>
- eSim/ngspice documentation: <https://esim.fossee.in>
- N. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective