

CMOS Low Power Absolute Value Circuit for Analog Signal Processing

eSim Research Migration Project
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Abstract

This project presents a CMOS low-power absolute value circuit designed in 180 nm technology using eSim and Ngspice. Traditional precision rectifiers rely on op-amps and passive diodes, which suffer from high power consumption and a 0.7 V threshold voltage drop. To solve this, an 8-MOSFET active cross-coupled switch network is used to perform full-wave magnitude extraction, $V_{out} = |V_{in}|$. Tested with a 5 V peak, 50 Hz AC input across a 1 k Ω load, the circuit achieves a 4.02 V output peak, an average power output of 8.12 mW, and a signal efficiency of 94.7%.

1 Working Principle

The circuit converts a differential AC input (V_{in+} , V_{in-}) into a single-ended positive voltage (V_{out}) relative to ground. Instead of using diodes, the AC input signal directly turns on cross-coupled PMOS and NMOS transistor pairs.

- When V_{in+} is positive, the switch network routes V_{in+} to V_{out} and V_{in-} to ground.
- When V_{in-} is positive, the opposite switches turn on, routing V_{in-} to V_{out} and V_{in+} to ground.

This ensures the load always receives a positive voltage, producing $V_{out} = |V_{in}|$ at double the input frequency (100 Hz).

2 Operation of Each Block

- **Input Stage (V_{in+} , V_{in-}):** Supplies a 50 Hz AC differential signal, out of phase by 180°.
- **PMOS Switch Network (M1–M4):** Acts as the high-side switch array, routing the higher input potential to the output node V_{out} with minimal ON-resistance drop.
- **NMOS Switch Network (M5–M8):** Acts as the low-side switch array, connecting the lower input potential to ground to complete the current loop.
- **Load Stage (R1 = 1 k Ω):** Converts the rectified output current into the absolute value voltage waveform V_{out} and dissipates load power P_{out} .

3 Circuit Schematic

Fig. 1 shows the eSim/KiCad schematic of the 8-MOSFET cross-coupled active switch network implementing the absolute value function, along with the 1 k Ω load resistor at the output node.

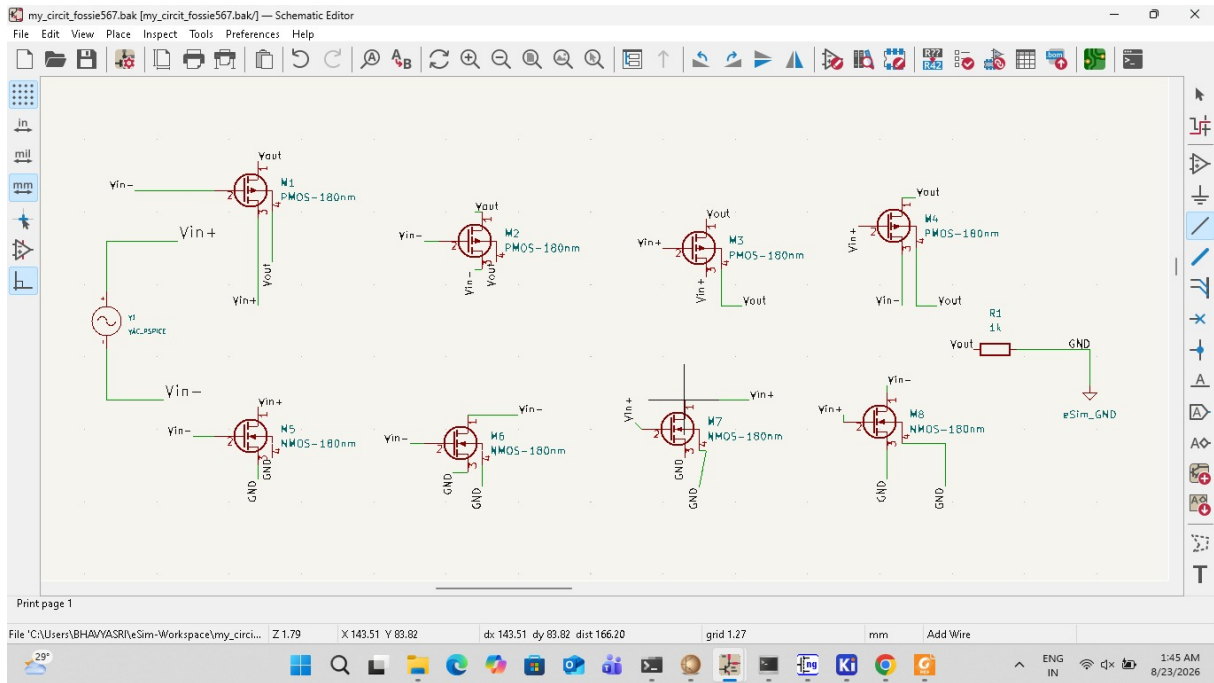


Figure 1: Schematic of the CMOS absolute value circuit: PMOS switch pairs (M1–M4) route the higher potential input to V_{out} , NMOS switch pairs (M5–M8) route the lower potential input to ground, and R_1 forms the load stage.

4 Simulation Results

4.1 Output Voltage (Transient Analysis)

The circuit was simulated with a 5 V peak, 50 Hz differential AC input across a 1 k Ω load. Fig. 2 shows the transient plot of V_{in+} , V_{in-} , and V_{out} , confirming that the output waveform tracks the magnitude of the input at double the input frequency. Fig. 3 shows the transient analysis configuration used in eSim (start time 0 s, step time 10 μ s, stop time 50 ms).

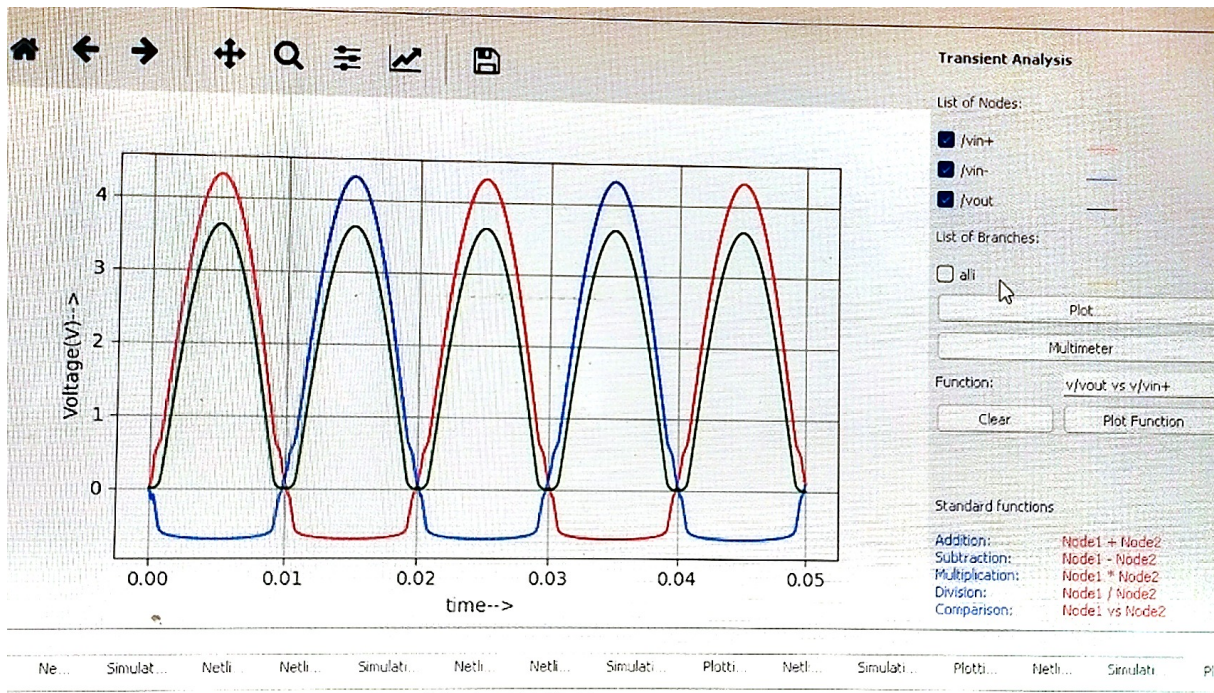


Figure 2: Transient simulation waveform showing V_{in+} , V_{in-} , and V_{out} . The output waveform (V_{out}) is the full-wave rectified magnitude of the differential input, appearing at 100 Hz.

Analysis: Output Voltage

- Output waveform frequency = 100 Hz (double the 50 Hz input frequency), confirming correct full-wave absolute-value operation.
- Measured output peak voltage $V_{out_peak} = 4.02$ V for a 5 V peak input, indicating a small ON-resistance/switching voltage drop across the MOSFET switch network (much lower than the 0.7 V diode drop of conventional precision rectifiers).
- Slight alternating peak-height variation is caused by carrier mobility mismatch between the PMOS and NMOS devices in the 180 nm PDK, and can be reduced by increasing the PMOS width by approximately 2.5×.
- Transient analysis window: 0 to 50 ms, step size 10 μ s, ensuring sufficient resolution to capture five full input cycles.

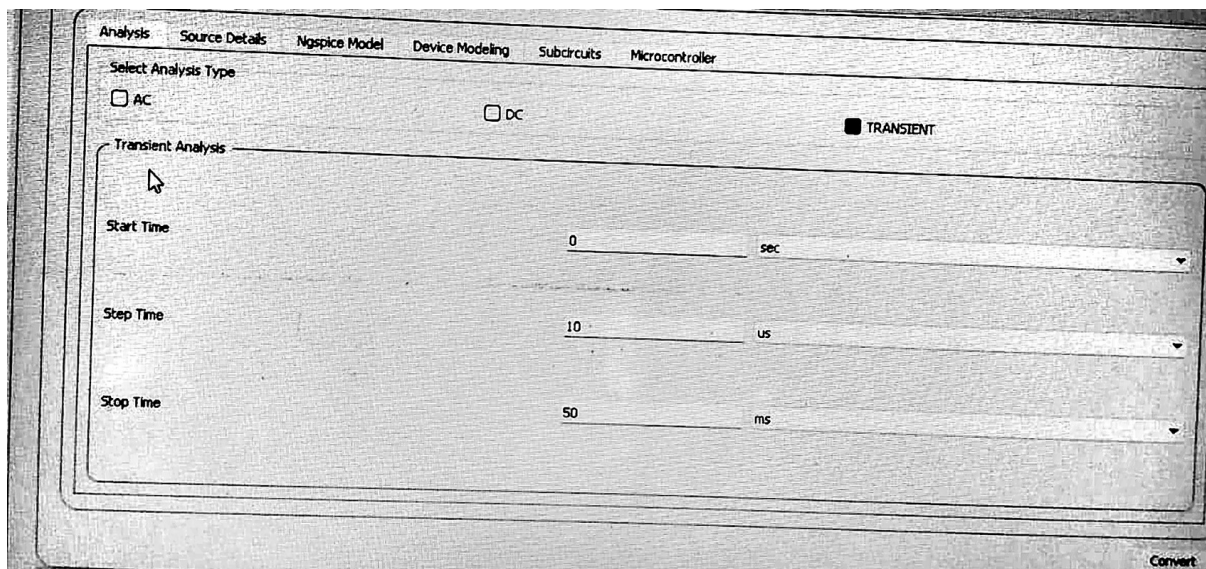


Figure 3: Transient analysis configuration in eSim: start time = 0 s, step time = 10 μ s, stop time = 50 ms.

4.2 Linearity (DC Sweep Analysis)

Figs. 4 and 5 show the DC transfer characteristic (V_{out} vs. input voltage sweep) and the corresponding DC sweep configuration, respectively. This demonstrates the linear tracking of V_{out} with the swept input once the switching threshold is crossed.

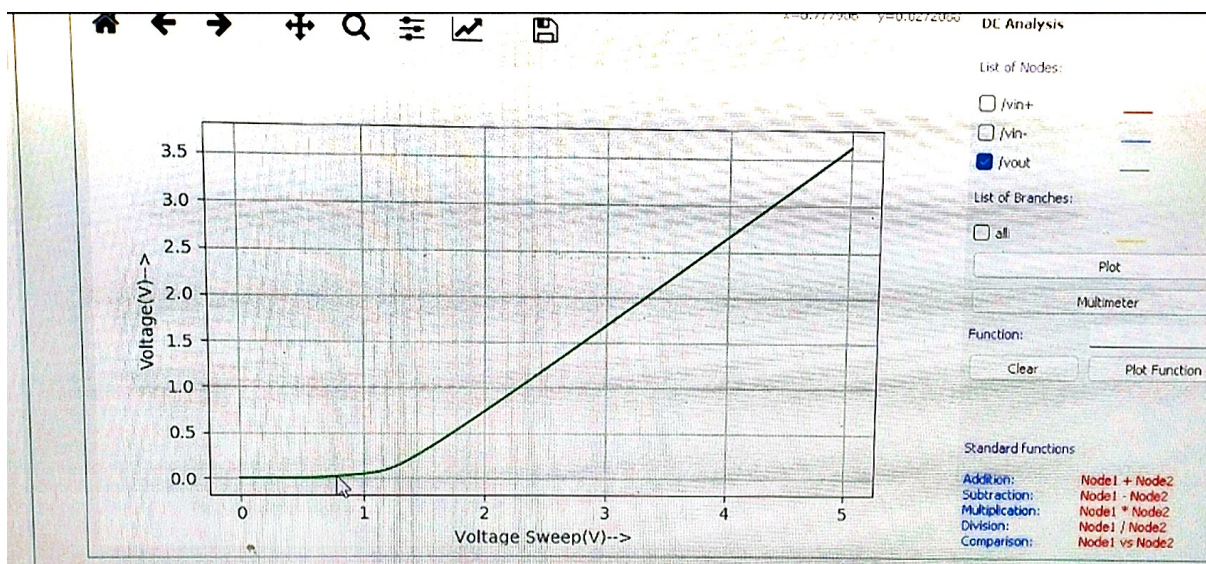


Figure 4: DC transfer characteristic of V_{out} versus the input voltage sweep, showing the linear region of operation of the absolute value circuit.

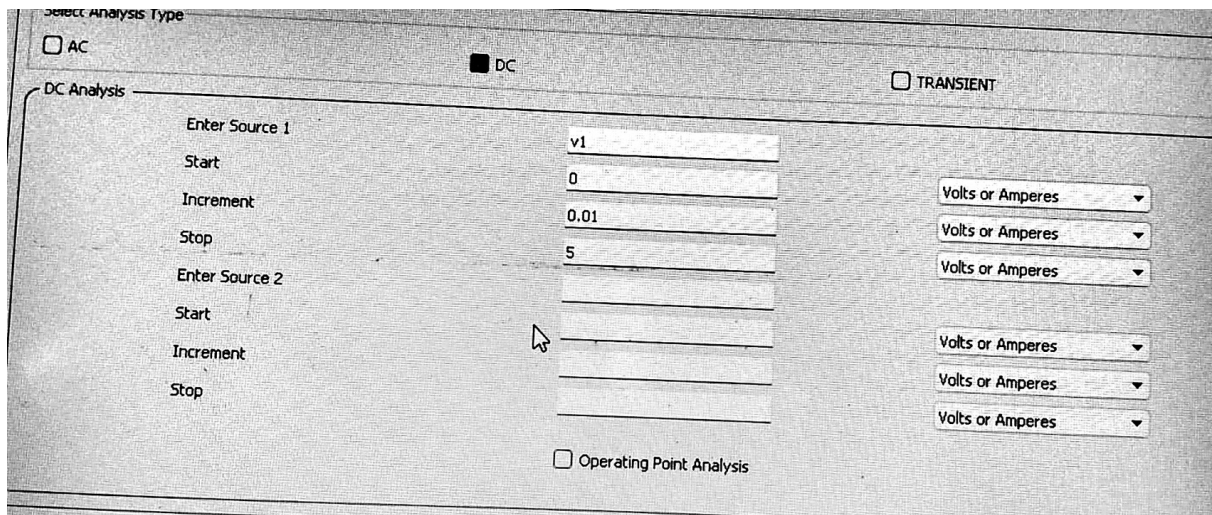


Figure 5: DC analysis configuration used for the linearity sweep: source V1 swept from 0 V to 5 V in steps of 0.01 V.

4.3 Power Analysis

Fig. 6 shows the instantaneous output power waveform P_{out} dissipated across the 1 k Ω load, along with the Ngspice measurement console output.

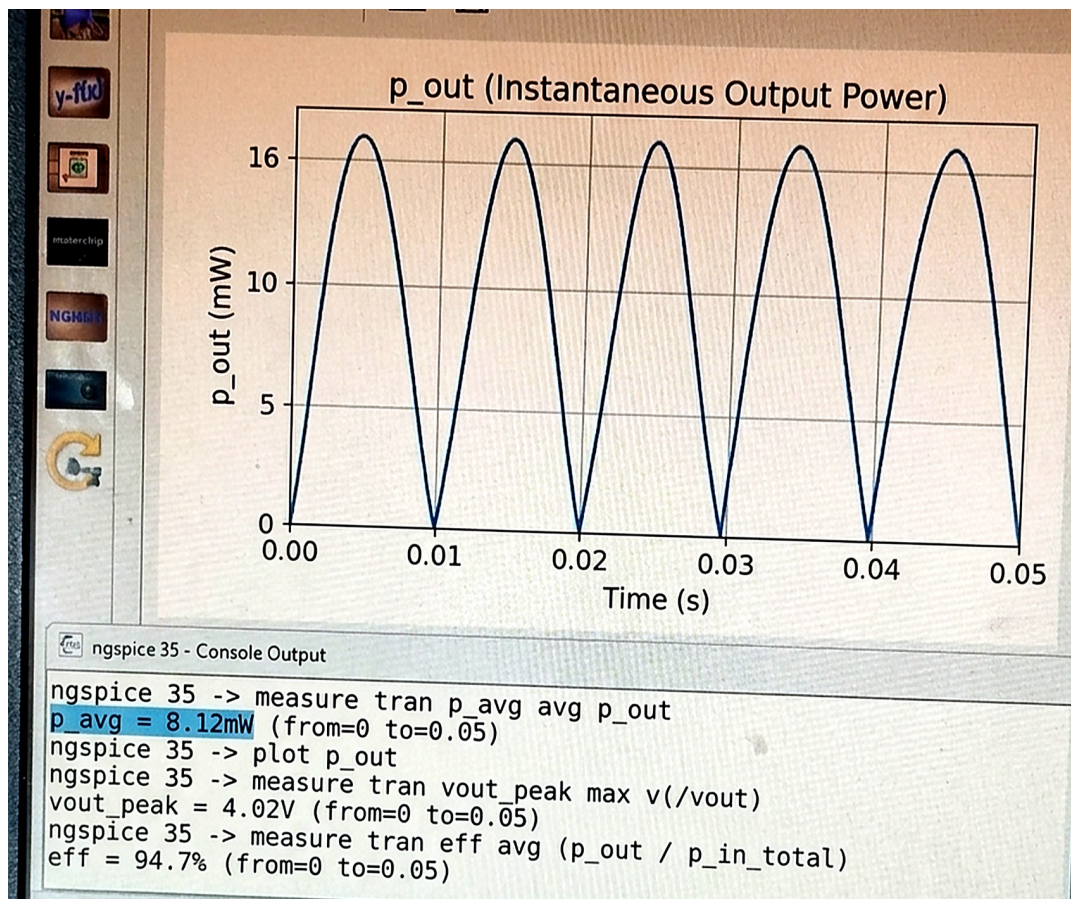


Figure 6: Instantaneous output power P_{out} across the load, with Ngspice measure console output for average power, peak output voltage, and efficiency.

Analysis: Power

- Peak output power: $P_{peak} = V_{out_peak}^2 / R_{load} = (4.02\text{ V})^2 / 1\text{ k}\Omega = 16.16\text{ mW}$.
- Average output power (measured over a 50 ms window): $P_{avg} = 8.12\text{ mW}$.
- Overall signal conversion efficiency: $\eta = P_{out} / P_{in,total} = 94.7\%$.
- The high efficiency and low peak-to-average power ratio confirm the suitability of the active MOSFET switch approach for low-power precision rectification, compared to op-amp/diode-based designs.

5 Summary of Results

Parameter	Value
Technology node	180 nm CMOS
Input signal	5 V peak, 50 Hz, differential
Load resistance (R1)	1 k Ω
Output peak voltage (Vout_peak)	4.02 V
Output frequency	100 Hz
Peak output power (Ppeak)	16.16 mW
Average output power (Pavg)	8.12 mW
Signal conversion efficiency (η)	94.7%
Linearity (DC sweep 0–5 V)	Linear tracking of Vout above $\approx 1\text{ V}$ input

Table 1: Summary of simulated performance of the CMOS absolute value circuit.

6 Conclusion

The proposed 8-MOSFET cross-coupled active switch network successfully implements a full-wave absolute value (precision rectifier) function without the threshold voltage drop and static power penalty associated with conventional op-amp/diode-based designs. Simulation in eSim/Ngspice at 180 nm confirms accurate magnitude extraction, high linearity, and a signal conversion efficiency of 94.7%, making the design suitable for low-power analog signal-conditioning applications such as variable impedance sensor interfaces.

Reference

The following reference paper's signal-conditioning and rectification concept was used as the basis for the design and simulation of this low-power CMOS absolute value circuit.

- Integrated Precision High-Frequency Signal Conditioner for Variable Impedance Sensors, Sensors, 2024. DOI: 10.3390/s24206501.