

Performance Analysis of a High Gain Non Isolated Hybrid Zeta Converter in Buck and Boost Modes

Research Migration Project Abstract

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Tool chain	eSim 2.5, KiCad 6.0.11, ngspice 35	Source	Electronics 2022, 11(3), Article 483
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Theory and Description:

The reference paper presents a high-gain non-isolated hybrid Zeta DC-DC converter in which two switching paths are controlled independently to obtain buck or boost operation. The common power stage contains two active switches, two power diodes, two inductors, an energy-transfer capacitor, an output capacitor and a resistive load. This research migration implements both operating modes in eSim and compares their transient and steady-state responses with the analytical, MATLAB/Simulink and OPAL-RT hardware-in-the-loop results reported by Reddy et al.

The steady-state relations used for validation are:

$$V_{C1} = \frac{V_{in}D_1}{1-D_1} \quad (8)$$

$$\frac{V_{out}}{V_{in}} = \frac{D_1^2}{1-D_1} + D_2 \quad (10)$$

where D_1 and D_2 are the switch duty ratios. The eSim model uses $V_{in} = 36$ V, $f_s = 10$ kHz, $L_1 = L_2 = 1$ mH, $C_1 = 100$ microfarads, $C_0 = 10$ microfarads and $R_0 = 30$ ohm. Parasitic and blocking elements are represented explicitly.

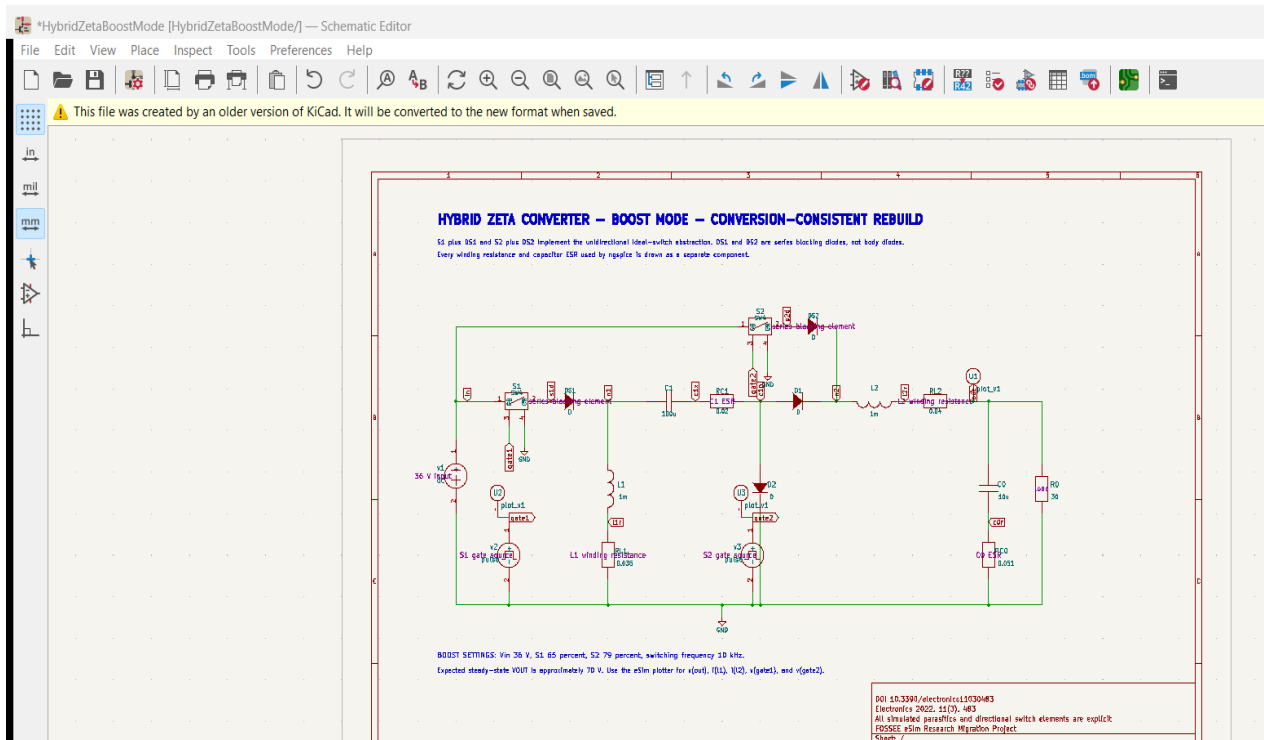
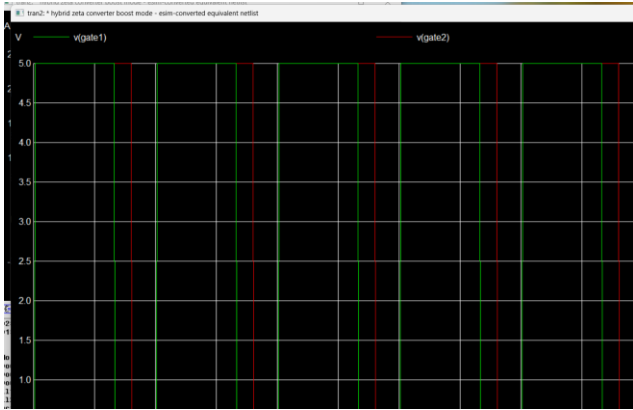


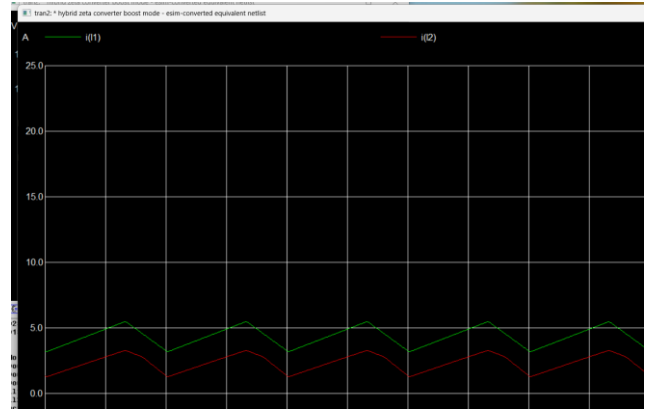
Figure 1. eSim/KiCad implementation of the hybrid Zeta power stage, including the explicitly modelled parasitic and blocking elements

Circuit 1: Boost Operating Case

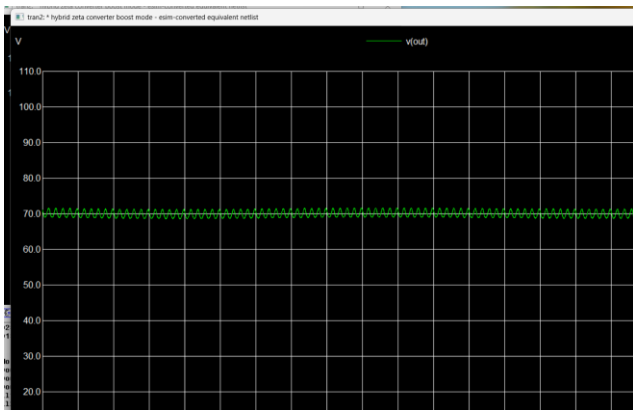
Published duties $D1 = 0.65$ and $D2 = 0.79$; $V_{in} = 36$ V; 10 kHz; $R0 = 30$ ohm



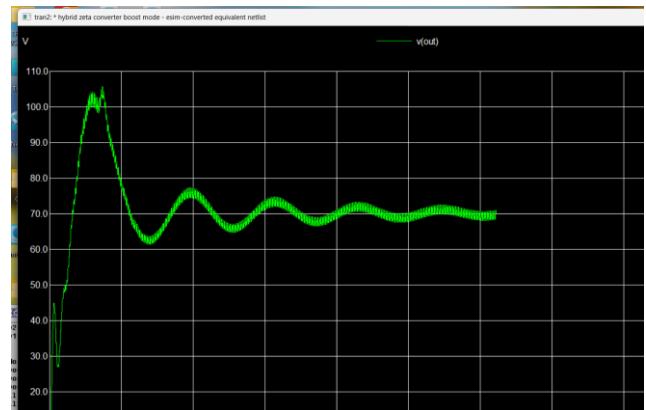
Gate pulses



Inductor currents



Steady-state output voltage



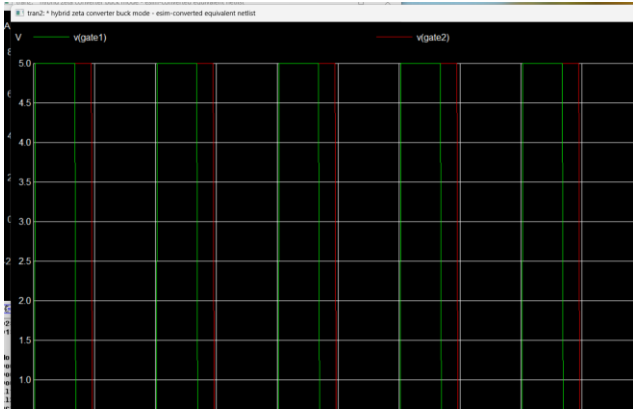
Startup and settling output voltage

Quantity	Published value	eSim result	Comparison
Average V_{out}	71.897 V by Equation 10; 70 V HIL	69.995 V	-2.645% from Equation 10; -0.007% from HIL
V_{out} range	Not tabulated	68.642 to 71.658 V	3.016 V peak-to-peak ripple
Average I_{L1}	4.68 A HIL	4.278 A	-8.58% from HIL
Average I_{L2}	2.04 A HIL	2.333 A	+14.37% from HIL
Average V_{C1}	66.857 V by Equation 8	65.542 V	-1.967% from Equation 8
Output-current balance	$I_{out} = V_{out}/R0$	I_{out} 2.333171 A; I_{L2} 2.333132 A	0.00167% difference

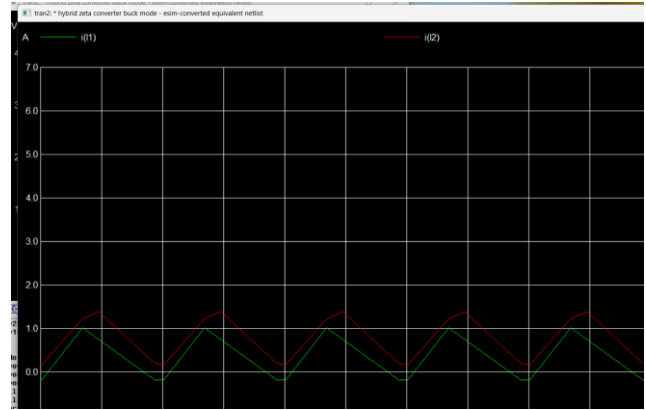
The eSim simulation yields 69.995 V, only 0.007% below the 70 V HIL result and 2.645% below Equation 10. $V_{out}/R0$ matches average I_{L2} within 0.00167%, confirming output-node current balance. Average I_{L1} and I_{L2} differ from HIL by -8.58% and +14.37%; therefore, agreement is strongest for voltage conversion and output-current consistency.

Circuit 2: Buck Operating Case

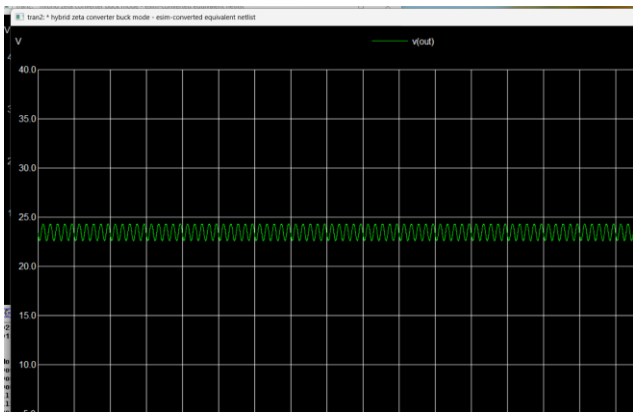
D1 = 0.33 published; D2 = 0.4625 inferred from Equation 10; Vin = 36 V; 10 kHz; R0 = 30 ohm



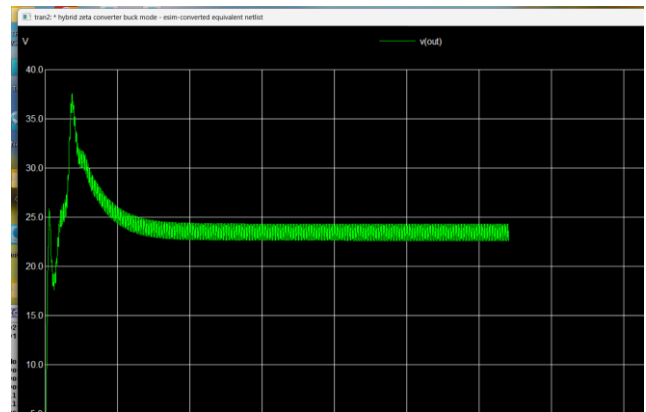
Gate pulses



Inductor currents



Steady-state output voltage



Startup and settling output voltage

Quantity	Published value	eSim result	Comparison
Average Vout	22.501 V by Equation 10; 22.6 V HIL	23.488 V	+4.383% from Equation 10; +3.928% from HIL
Vout range	Figure 7 visually near 24 V	22.613 to 24.314 V	Consistent with the plotted waveform
Output current	Figure 7 near 0.8 A; HIL 0.760 A	0.782921 A	Consistent with plotted and HIL output currents
Average IL1	HIL maximum about 1.61 A; average reporting is ambiguous	0.371 A; minimum -0.195 A	Internal-current agreement not obtained; CCM not established
Average IL2	HIL maximum about 1.63 A; average reporting is ambiguous	0.782921 A	Matches the average load current
Average VC1	17.731 V by Equation 8; 14 V HIL text	19.373 V	+9.257% from Equation 8

The paper specifies D1 = 0.33 for buck operation but omits D2. Here, D2 = 0.4625 is inferred from Equation 10 using the stated 22.5 V target. The eSim model yields 23.488 V and 0.783 A, consistent with Figure 7 and within 3.928% of the 22.6 V HIL result. Since 22.5 V across 30 ohm implies 0.75 A, the paper's separate 2 A statement is treated as inconsistent.

Accuracy, Complexity and Independent Validation

Quantitative validation:

Validation parameter	Boost	Buck
Operating case	D1 0.65, D2 0.79 published	D1 = 0.33 published; D2 = 0.4625 inferred from Equation 10
Equation 10 Vout	71.897 V	22.501 V
Average Vout from ngspice	69.995 V	23.488 V
Output-current balance	2.333171 A versus 2.333132 A	0.782921 A versus 0.782921 A
Steady-state window	40 ms to 50 ms	40 ms to 50 ms
Recorded waveforms	Gate pulses, currents, startup Vout and steady-state Vout	Gate pulses, currents, startup Vout and steady-state Vout
Simulation integrity	Clean run; valid time-indexed plot data	Clean run; valid time-indexed plot data

Sensitivity analysis:

Case	Equation 10	ngspice result	Interpretation
Buck D2 = 0.4625	22.501 V	23.488 V	Selected equation-derived buck operating point
Buck D2 = 0.531907	25.000 V	25.099 V	+0.396% relative to the analytical 25 V value
Direct bidirectional switch, boost	71.897 V	28.371 V; IL1 about 190.6 A	Unrealistic circulating current; model excluded
Direct bidirectional switch, buck	22.501 V	15.826 V; IL1 about 36.3 A	Unrealistic circulating current; model excluded

Sixteen supplementary ngspice cases examined duty-ratio and switch-model sensitivity; all completed without warnings or missing measurements. Fresh runs of both projects produced valid time-indexed data and the stated output averages. The direct bidirectional switch was excluded because it caused unrealistic circulating currents, whereas series blocking diodes preserved the intended power-flow direction.

Implementation scope

The eSim model retains the two controlled paths, power and blocking diodes, winding resistances, capacitor ESRs and load. Relevant nodes are labelled for transient measurement, and device models are stored locally. The boost and buck projects use the same published power stage and can be opened, converted and simulated independently.

Reproducibility, Limitations and Reference

Running the eSim projects:

1. Extract the archive and use Open Project in eSim to select HybridZetaBoostMode or HybridZetaBuckMode. Select the directory containing the matching .proj file, not the archive root or a results folder.
2. If the project has been moved, reselect the three project-local model .lib files in the eSim converter before regenerating the netlist.
3. Open the KiCad schematic and verify the component values, node labels and model assignments.
4. Run Convert KiCad to Ngspice, confirm the stored source, model and transient-analysis settings, and select Convert.
5. Run Simulation. Native ngspice windows display output voltage, inductor currents and gate pulses; eSim also generates time-indexed plot-data files.

Project-directory contents:

Directory	Principal files and purpose
HybridZetaBoostMode	Matching .proj, .pro, .sch, .bak, .cir and .cir.out files; analysis settings, cache files, model XML and project-local .lib files
HybridZetaBuckMode	Independent files for $D1 = 33\%$ and Equation-10-derived $D2 = 46.25\%$
Device models	HybridZetaSwitch.lib, HybridZetaBlockingDiode.lib and HybridZetaPowerDiode.lib, with corresponding eSim Model Builder XML records

Limitations:

1. The controlled-switch model supports voltage-transfer analysis, not manufacturer-specific loss, device-stress or efficiency estimates.
2. Because $D2$ is omitted and the buck data are inconsistent, $D2$ is inferred and internal-state agreement remains limited.
3. Buck $IL1$ becomes slightly negative; continuous-conduction operation is therefore not claimed for this case.
4. Boost output voltage agrees closely with HIL, while average inductor-current agreement is partial.

Conclusion: The hybrid Zeta converter was implemented in eSim as separate boost and buck projects. Boost operation gives 69.995 V, closely matching the 70 V HIL result. The inferred buck duty gives 23.488 V, within 3.928% of HIL. Output-current balance is satisfied in both modes. The migration reproduces voltage-transfer behaviour while documenting limitations of the simplified switch model and incomplete buck data.

Reference:

P. L. S. K. Reddy, Y. P. Obulesu, S. Singirikonda, M. Al Harthi, M. S. Alzaidi, and S. S. M. Ghoneim, "A Non-Isolated Hybrid Zeta Converter with a High Voltage Gain and Reduced Size of Components," Electronics, vol. 11, no. 3, Art. no. 483, pp. 1-17, 2022, doi: 10.3390/electronics11030483.