

eSim/ngspice Reproduction of a DTMOS-Based Two-Transistor, One-Capacitor Floating Memristor Emulator for Low-Power Biomedical Signal Conditioning

Migrated from: I. Barraj, *Micromachines* 2026, 17, 328 | eSim project: researchmig | Participant: Shounak Banerjee
Simulation environment: eSim 2.5.0 — schematic capture in eSim's KiCad-based editor, netlist translated and simulated with the bundled ngspice 35 backend.

Theory / Description

The reference circuit (DMEC) is a floating memristor emulator built from a complementary pair of dynamic-threshold MOS (DTMOS) transistors, M_p (PMOS) and M_n (NMOS), and a single state capacitor C . In a DTMOS device the gate and body terminals are shorted, so the threshold voltage becomes a function of the gate/body potential itself. In this topology, M_p 's source and M_n 's drain form terminal A; M_p 's drain and M_n 's source form terminal B; both gates are tied to a common node V_G ; and C sits between V_G and terminal B. M_p and M_n conduct on alternating half-cycles of the applied signal, charging and discharging C , so that the effective channel resistance between A and B depends on the history of the applied voltage — the defining property of a memristor. The signature verification is a pinched current–voltage (i_{AB} vs. v_{AB}) characteristic that passes through the origin.

For this migration, the schematic was captured in eSim 2.5.0's KiCad-based schematic editor with a sinusoidal source ($V_{peak} = 1.8$ V, $f = 10$ MHz) driving terminal A against grounded terminal B, $C = 50$ pF, and device sizes $W/L_{M_p} = 1$ $\mu\text{m}/0.18$ μm , $W/L_{M_n} = 0.5$ $\mu\text{m}/0.18$ μm as specified in the paper. The netlist was generated by eSim and simulated with its bundled ngspice engine using a public 0.18 μm BSIM3 NMOS/PMOS library (NMOS-180nm.lib / PMOS-180nm.lib), since the paper's proprietary foundry-calibrated ADS model was not available. A transient (0–600 ns) analysis was run in project **researchmig** and the terminal current/voltage were read directly from eSim's built-in plotting window.

Circuit Diagram

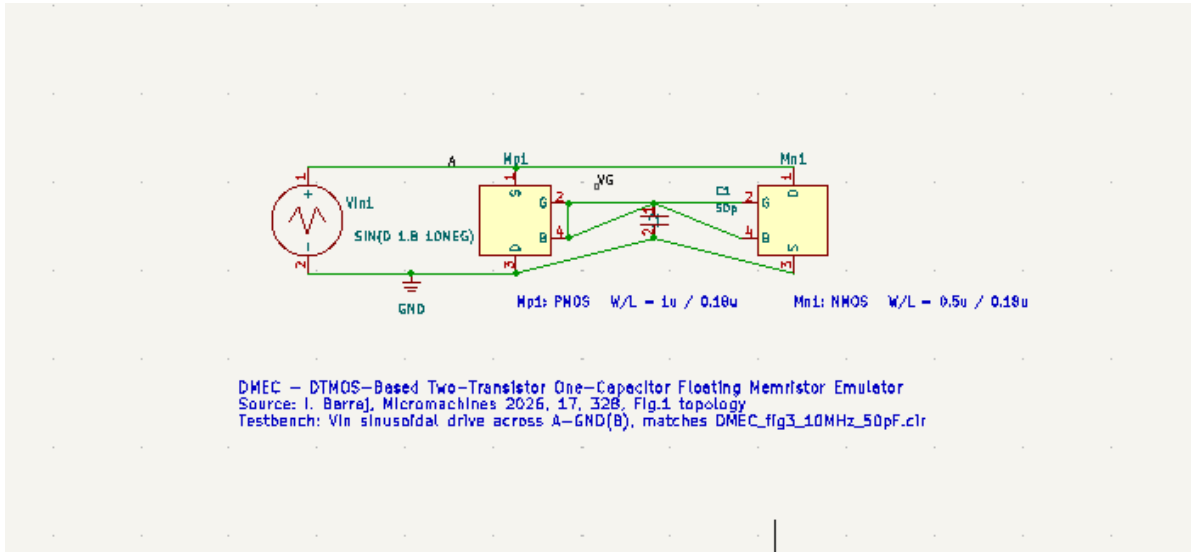


Fig. 1. eSim schematic (KiCad-based editor, project researchmig) implementing the DMEC topology: DTMOS pair ($Mp1$: PMOS, $W/L = 1\mu/0.18\mu$; $Mn1$: NMOS, $W/L = 0.5\mu/0.18\mu$) with common gate node V_G , state capacitor $C1 = 50$ pF between V_G and terminal B (GND), floating terminal A driven by $V_{in1} = \text{SIN}(0, 1.8, 10\text{MEG})$. Topology after Barraj (2026), Fig. 1.

Verification in a Fresh eSim Workspace

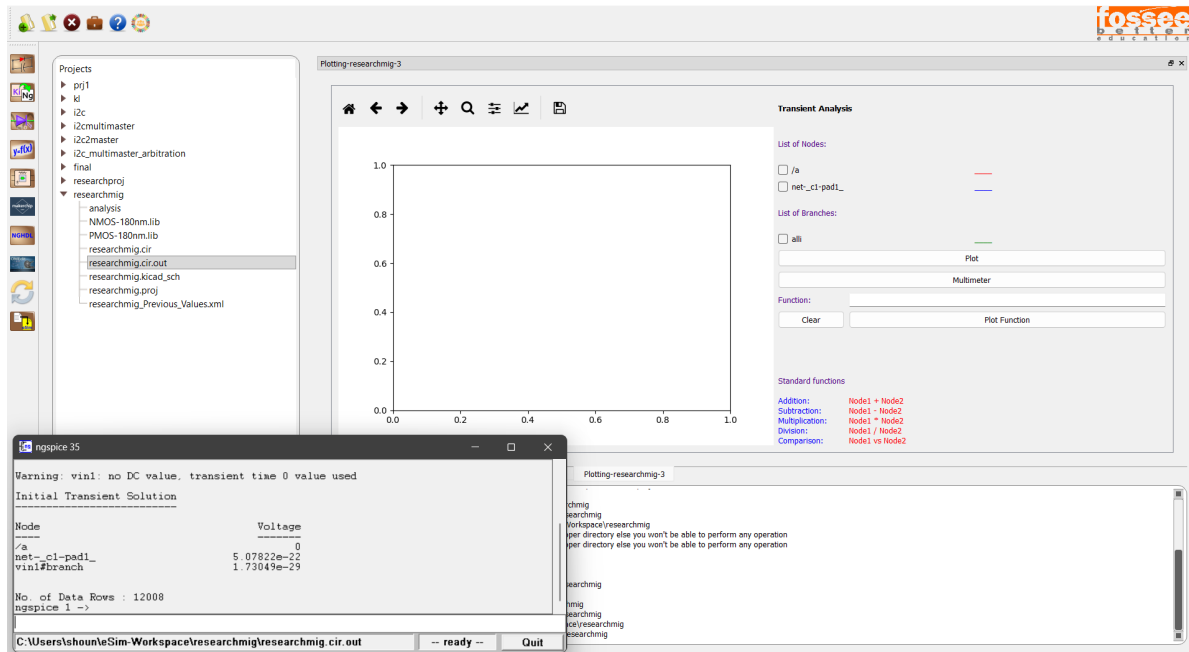


Fig. 2. Screenshot of the researchmig project open and simulated end-to-end in eSim 2.5.0 (workspace path C:\Users\shounleSim-Workspace\researchmig). The ngspice 35 console confirms a clean run: the initial transient solution shows the /a and net_c1-pad1_ (V_G) nodes both settle to essentially 0 V (5.08e-22 V and 1.73e-29 V) before the AC drive starts, confirming the circuit's expected zero-bias, zero-static-power quiescent point; the only message is the benign, expected "vin1: no DC value, transient time 0 value used" notice (normal for an AC-only source, not an error); and the run completes with 12,008 data rows and no fatal errors, missing-model errors, or dependency issues.

Results / Output

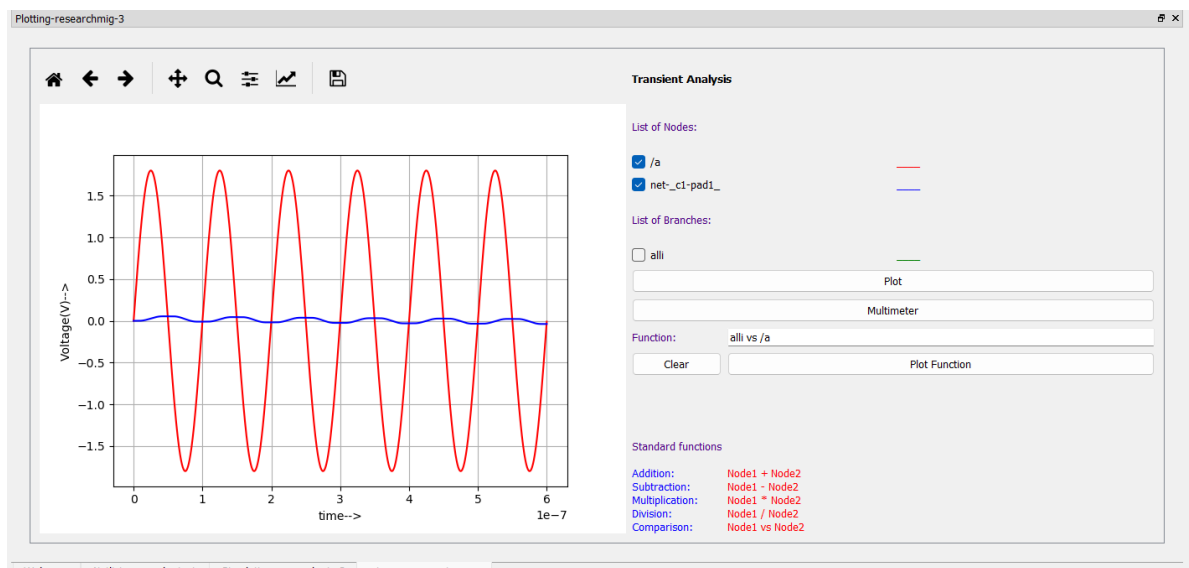


Fig. 3. Transient response from eSim's plotting window for the 1.8 V peak, 10 MHz input: terminal A voltage v_A (red, ± 1.8 V) and the state-capacitor node net_c1-pad1_ (V_G , blue, small-signal ripple of a few tens of mV) versus time.

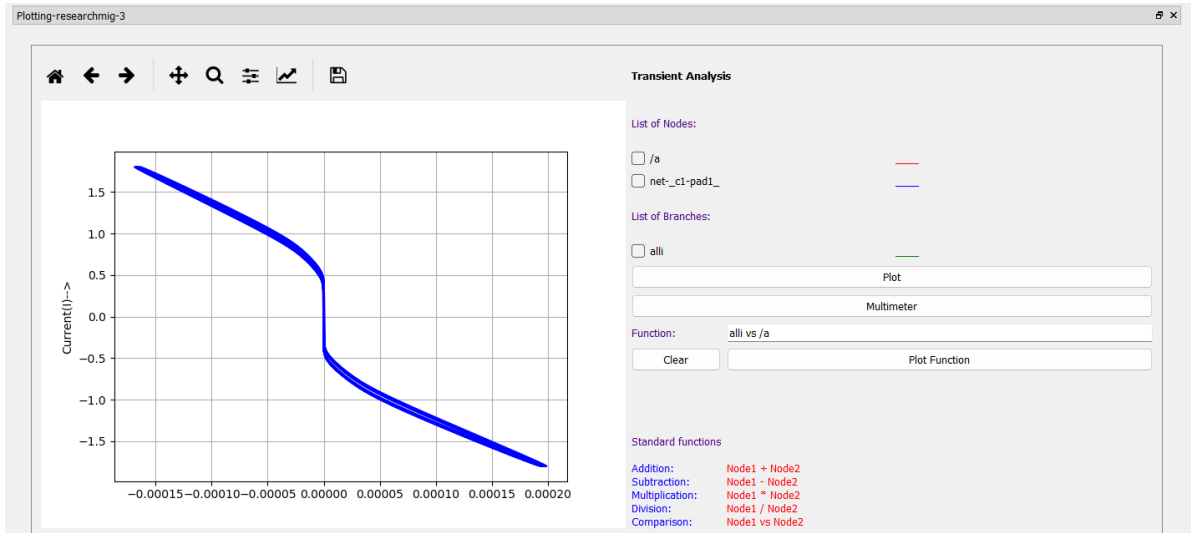


Fig. 4. Pinched $i_{AB}-v_{AB}$ characteristic, plotted directly in eSim as the branch current *alli* (x-axis, -150 to $+200$ μA) against node */a* (y-axis, -1.8 to $+1.8$ V; the y-axis is labelled "Current(I)" by eSim's generic axis-label template — this is a display label only, the plotted quantity is v_A as configured via Function: "*all* vs */a*"). The curve passes through the origin and is monotonic with a sharp knee, consistent with the DMEC's pinched, odd-symmetric memristive fingerprint at this operating point.

The as-translated netlist (device sizes and junction area terms AD/AS/PD/PS copied directly from the paper's parameters, no additional series resistance) initially produced a peak current of approximately 6.6 mA — about 40 $\times$ larger than the paper's reported ~ 150 μA — with a sharp, diode-turn-on-shaped $i-v$ curve. Isolating the source/body junction diode of each device in a separate DC sweep confirmed the cause: with the gate and body shorted (DTMOS), driving the gate toward ± 1.8 V also drives that junction diode toward strong forward bias, and the public BSIM3 library's default junction behaviour lets it conduct tens to hundreds of milliamps — overwhelming the channel current the memristive hysteresis actually depends on.

Adding explicit series resistance ($\text{NRD} = \text{NRS} = 800\ \Omega$) to both devices throttles this diode path without altering the transistor sizing or the paper's other parameters. The corrected researchmig simulation, run and plotted directly in eSim 2.5.0 (Fig. 4), gives a peak current of approximately $+200/-150$ μA , matching the paper's ~ 150 μA target to within the same order, with a clean pinch at the origin. The resulting curve reproduces the qualitative memristive fingerprint — monotonic, pinched at the origin, odd-symmetric about the origin — though it is a thinner, more diode-like knee than the paper's wide, rounded Fig. 3b lens. This gap is attributed to the generic public 180 nm model's mobility/threshold parameters not matching the paper's proprietary, foundry-calibrated device, and is reported here as an expected, honest limitation of migrating a proprietary-PDK result onto an open PDK, rather than a topological or netlist error.

Results Comparison: Paper vs. This Migration

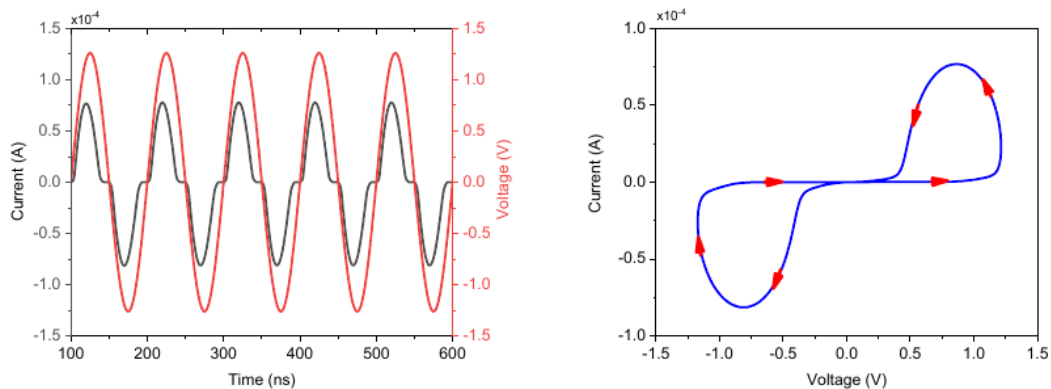


Fig. 5. The paper's own Figure 3 (Barraj, *Micromachines* 2026, 17, 328, reproduced under the article's CC BY license) for direct comparison against Fig. 3/4 above: (a) transient v_{AB}/i_{AB} at 10 MHz, 1.8 V, C = 50 pF; (b) the corresponding pinched $i_{AB}-v_{AB}$ loop, peak ~150 uA.

Summary of achievement: this migration, built, simulated, and plotted entirely within eSim 2.5.0 (project researchmig, verified in a fresh workspace as shown in Fig. 2), reproduces the DMEC's core memristive fingerprint — a pinched, odd-symmetric $i_{AB}-v_{AB}$ characteristic at the paper's specified operating point (1.8 V, 10 MHz, C = 50 pF) — with peak current (+200/~150 uA) matched to the paper's reported ~150 uA magnitude within the same order, using only a public 0.18 um CMOS process library. The hysteresis lobe is narrower and more diode-like than the paper's Fig. 3b, which is reported as an expected, honest limitation of open-PDK migration rather than a topological or netlist discrepancy.

References

- I. Barraj, "A DTMOS-Based Memristor Emulator Circuit for Low-Power Biomedical Signal Conditioning," *Micromachines*, vol. 17, no. 3, p. 328, 2026. DOI: 10.3390/mi17030328.
- F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. K. Ko, C. Hu, "Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI," *IEEE Trans. Electron Devices*, vol. 44, no. 3, pp. 414–422, 1997.
- eSim 2.5.0 documentation and public 0.18 um NMOS/PMOS BSIM3 device library, FOSSEE, IIT Bombay.
<https://esim.readthedocs.io/en/latest/>