

Fast Switched CMOS Inverter using 180nm VLSI Technology

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Abstract

This report documents the outcomes of a research migration project conducted by FOSSEE, wherein the electronic circuits and simulations of a research paper titled ***Investigation of Fast Switched CMOS Inverter using 180nm VLSI Technology*** were successfully replicated using the open- source EDA tool **eSim**, utilizing the default eSim library models under **180nm technology**. The original simulations presented in the paper were performed in Cadence Virtuoso.

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1 Introduction and Theory

1.1 Introduction

The CMOS inverter comprises complementary nMOS and pMOS transistors which is the digital design core of efficient switching due to low-power dissipation; high noise immunity; and nearly zero static consumption. The pMOS (W/L) ratio is set to nearly 2.5 times compared to nMOS for balanced operation. This gives a versatile building block that tends to simplify more complex digital designs, such as NAND and NOR gates, which also form the nucleus of processors and of complex systems themselves.

1.2 Theory

The CMOS inverter, a fundamental component in digital circuits, operates using complementary nMOS and pMOS transistors. It switches between high (V_{DD}) and low (0V) output states based on the input voltage. To achieve balanced operation, the (W/L) ratio of pMOS is typically set 2–3 times larger than that of nMOS, compensating for the lower hole mobility of pMOS transistors.

Characteristics of nMOS and pMOS Transistors

MOSFET operation is classified into three modes:

1. **Cut-Off (Subthreshold) Mode:** when $V_{gs} < V_{th}$
2. **Linear (Triode) Mode:** when $V_{gs} > V_{th}$ and $V_{ds} < (V_{gs} - V_{th})$
3. **Saturation (Active) Mode:** when $V_{gs} > V_{th}$ and $V_{ds} > (V_{gs} - V_{th})$

For pMOS transistors, these modes are reversed with opposite voltage polarities. These characteristics define the transistor's switching and current behavior, essential for inverter performance.

DC Characteristics

The DC characteristics plot V_{out} against V_{in} , showcasing the voltage transfer curve (VTC). Ideally, the VTC is a sharp transition, but in practice, it features a gradual region where both transistors conduct. The switching threshold, where $V_{in} = V_{out}$, is a critical parameter. For optimal performance, this threshold is typically designed to be around $V_{DD}/2V$.

Transfer Characteristics

The transfer characteristics reflect the inverter's dynamic behavior during switching. As V_{in} transitions from low to high or vice versa, V_{out} changes inversely. The slope of the VTC in the transition region indicates switching precision—steeper slopes signify better performance. The width and length of transistors influence this slope, impacting the inverter's speed and power efficiency.

2 Design of CMOS

CMOS inverter has been implemented in 180nm technology with specification

1. DC voltage source to V_{DD} , $V_{dc}=V_{DD}=1.8V$
2. Common input pulse to Gate, V_{pulse} , V_1 (low level) =0V, V_2 (high level) = 1.8V,
3. Period=20ns, Delay=1ns, Rise time, t_r = 10ns, Fall time, t_f = 10ns, Pulse width= 10ns.

Transfer characteristics: stop time=200ns.

DC characteristics: sweep range = 0 to 1.8V.

After that, waveforms are plotted. Similarly, vary the width of pMOS and nMOS transistors, such that $(W/L)_p$ is approximately 2 to 3 times of $(W/L)_n$.

As

$$\beta = (\mu\epsilon/t_{ox})(W/L), [11] \quad (1)$$

For nMOS,

$$\beta_n = (\mu_n\epsilon/t_{ox})(W/L)_n, \quad (2)$$

pMOS,

$$\beta_p = (\mu_p\epsilon/t_{ox})(W/L)_p \quad (3)$$

In case of $(W/L)_p=(W/L)_n$ and same oxide thickness and permittivity,

Dividing (2) and (3), we get

$$\beta_n / \beta_p = (\mu_n / \mu_p)$$

As electron mobility, μ_n is approximately 2 to 3 times the mobility of holes, μ_p . Therefore, β_n should be 2 to 3 times β_p . For length to be equal, it can be concluded that W_p should be 2 to 3 times W_n for switching threshold to be optimum.

3 Circuit Diagrams

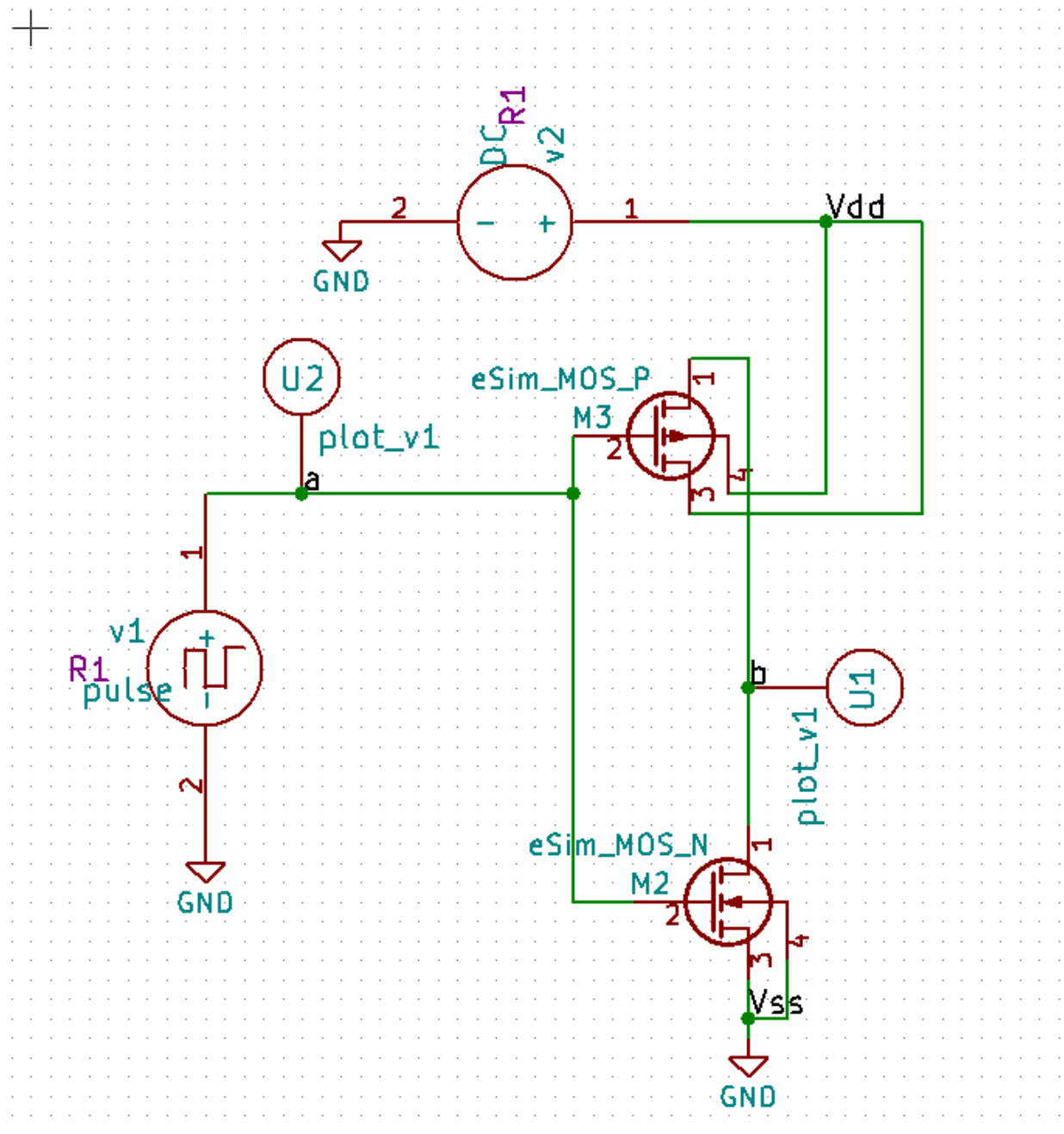


Figure 1: kiCad schematic

4 Output Plots

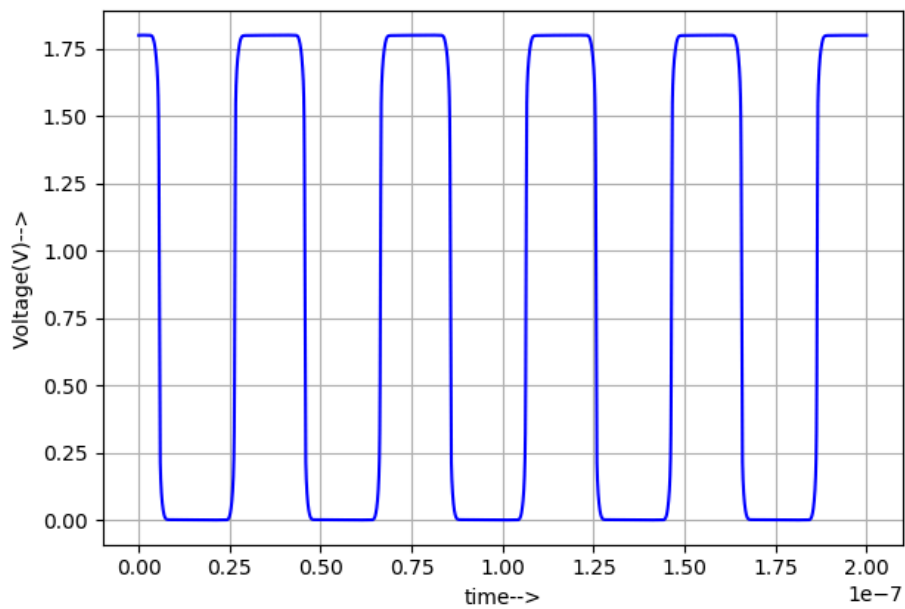
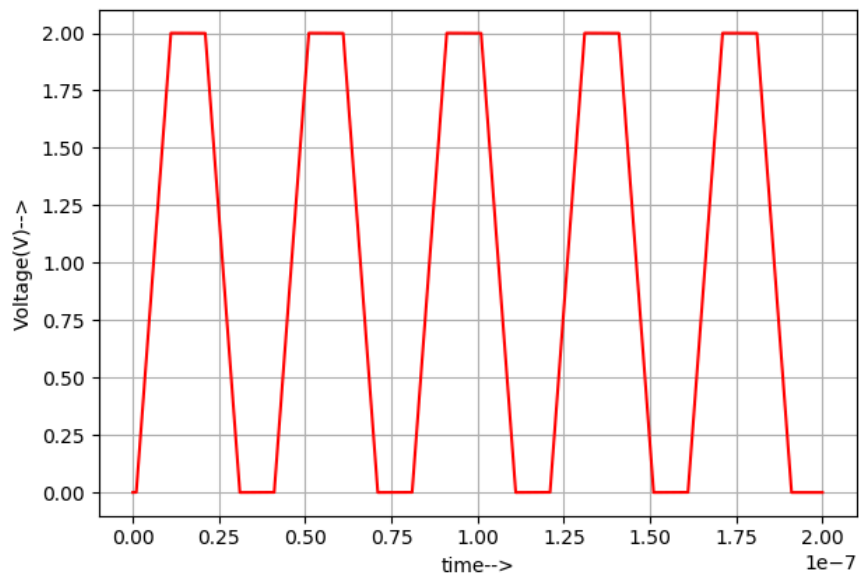


Figure 2 :Transient Analysis of CMOS Inverter

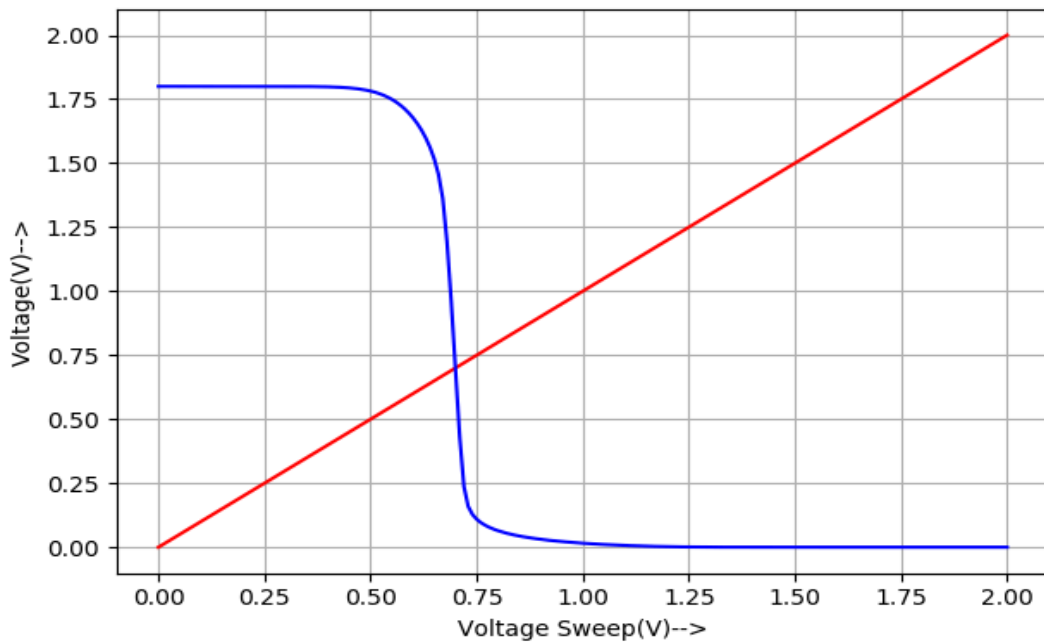


Figure 3 : DC Analysis of CMOS Inverter for $W_p / W_n = 0.4$

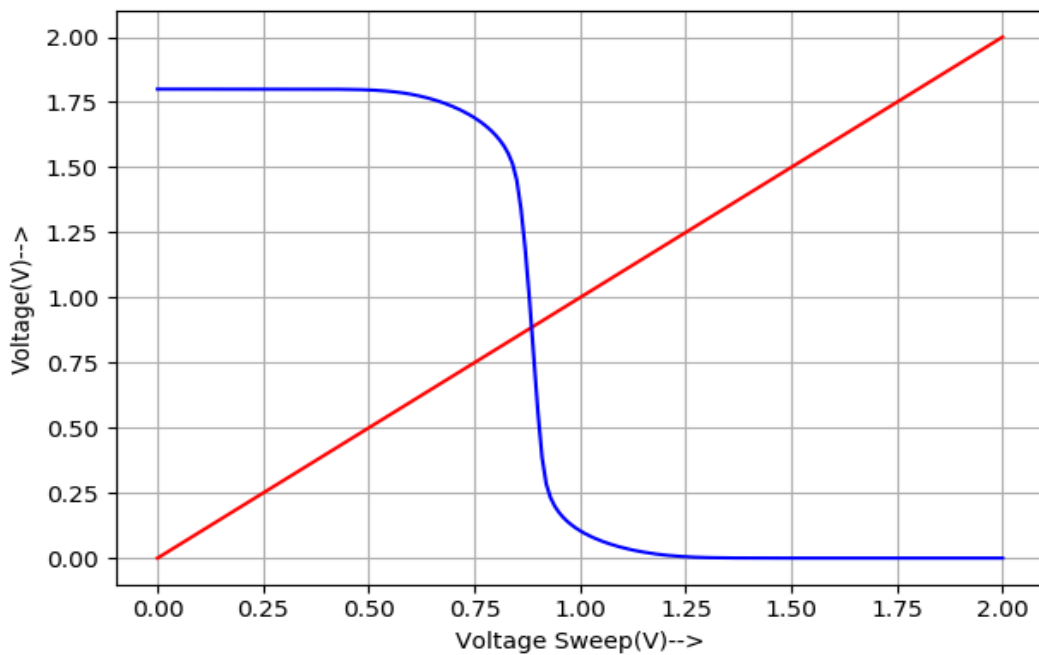


Figure 4 :DC Analysis of CMOS Inverter for $W_p / W_n = 2.5$

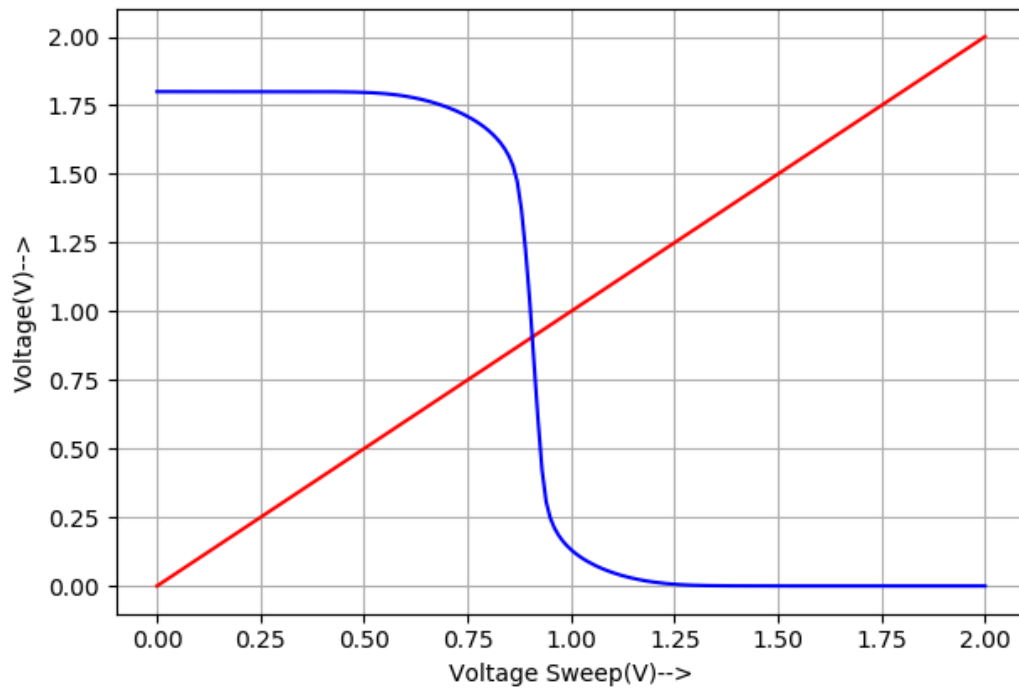


Figure 5 :DC Analysis of CMOS Inverter for $W_p / W_n = 3$

Sl No.	pMOS width $W_p(\mu m)$	nMOS width $W_n(\mu m)$	$(W/L)_p$	$(W/L)_n$	Switching Threshold
1	4	10	22.2	55.5	0.69
2	10	4	55.5	22.2	0.85
3	12	4	66.6	22.2	0.90

Table 1: Comparison of switching threshold with variation in W/L of pMOS and nMOS transistor ($L=180nm$)

5 Conclusion

The DC response of a CMOS inverter shows that when $W_p/W_n = 3$, the inverter switches between logic 1 and logic 0 at $V_{DD}/2$, which is ideal for inverter operation. In other cases, the switching point shifts to values like 0.69 or 0.85, which are less desirable. To ensure proper switching, the width of the pMOS transistor should be 2 to 3 times larger than that of the nMOS transistor.

Changing the W_p/W_n ratio affects the switching point of the voltage transfer curve (VTC). Increasing the pMOS width moves the switching point closer to V_{DD} , while increasing the nMOS width shifts it closer to the ground. This behavior can be useful in designs where asymmetrical transfer characteristics are needed.

References

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