

Leveraging eSim for Switched Model Simulation of Control PWM Circuits in DC-DC Power Converters

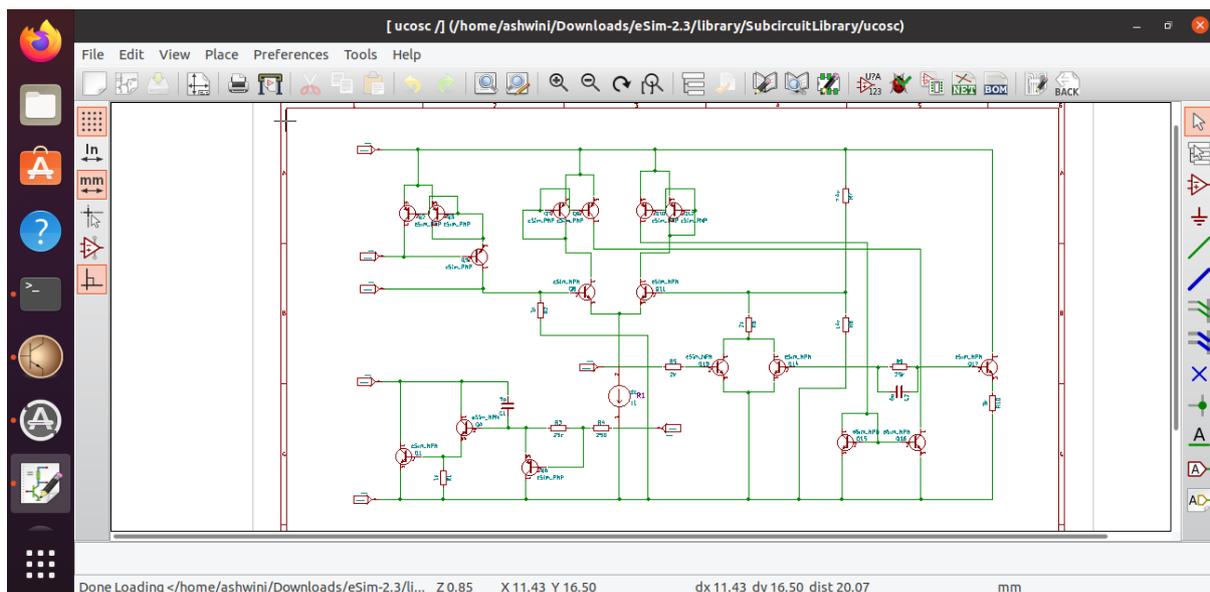
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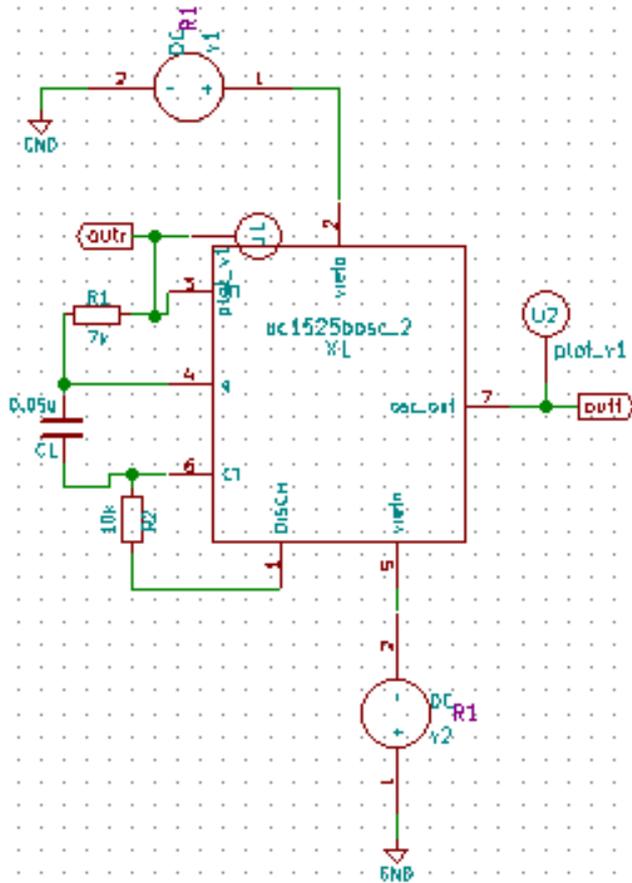
Abstract:

This paper focuses on two prominent modeling techniques for switch mode DC/DC power converters: between (a) the average model and (b) the switched model. The general case of the regular model uses the constant changing of the voltages or currents to that of the average switched model, which applies them for the fractional part of the commutation period. Here I will look into the switched model technique and its application in integrating power switches layout. The simulation model is designed using eSim simulation software, which acts as a powerful environment for circuit simulations and analysis. eSim being the link between the abstract circuit design and the practical implementation, the designers can shortcut the design process. This way, when surprises pop up, they can manage them. Modelling and simulation methods will be applied on popular control PWM Integrated Circuits UC 1525 and UC 1846. Different elements, including the oscillator, error amplifier, and comparator are designed and simulated with subcircuits.

Circuit Diagram:

UC1525 subcircuit oscillator:





Netlist generated from eSim:

* /home/ashwini/downloads/esim-2.3/library/subcircuitlibrary/ucosc/ucosc.cir

```
.include PNP.lib
.include NPN.lib
q2 net_q2-pad1_net_q2-pad2_net_q10-pad3_Q2N2907A
q3 net_q2-pad2_net_q2-pad2_net_q10-pad3_Q2N2907A
q5 net_q5-pad1_net_q2-pad1_net_q2-pad2_Q2N2907A
q7 net_q7-pad1_net_q7-pad1_net_q10-pad3_Q2N2907A
q9 net_q16-pad1_net_q7-pad1_net_q10-pad3_Q2N2907A
q10 net_q10-pad1_net_q10-pad2_net_q10-pad3_Q2N2907A
q12 net_q10-pad2_net_q10-pad2_net_q10-pad3_Q2N2907A
q8 net_q7-pad1_net_q5-pad1_net_i1-pad2_Q2N2222
q11 net_q10-pad2_net_q11-pad2_net_i1-pad2_Q2N2222
q13 net_q13-pad1_net_q13-pad2_net_i1-pad1_Q2N2222
q14 net_q13-pad1_net_c2-pad2_net_i1-pad1_Q2N2222
q15 net_q10-pad1_net_q10-pad1_net_i1-pad1_Q2N2222
q16 net_q16-pad1_net_q10-pad1_net_i1-pad1_Q2N2222
q17 net_q10-pad3_net_c2-pad1_net_q17-pad3_Q2N2222
q1 net_c1-pad2_net_q1-pad2_net_i1-pad1_Q2N2222
q4 net_c1-pad2_net_c1-pad1_net_q1-pad2_Q2N2222
q6 net_i1-pad1_net_q6-pad2_net_c1-pad1_Q2N2907A
r6 net_q11-pad2_net_q13-pad1_2k
r8 net_q11-pad2_net_i1-pad1_14k
r7 net_q10-pad3_net_q11-pad2_7.4k
r9 net_c2-pad2_net_c2-pad1_25k
```

```

c2 net-_c2-pad1_net-_c2-pad2_6p
r10 net-_q17-pad3_net-_i1-pad1_3k
i1 net-_i1-pad1_net-_i1-pad2_dc 0.4m
r3 net-_c1-pad1_net-_q6-pad2_23k
c1 net-_c1-pad1_net-_c1-pad2_5p
r1 net-_q1-pad2_net-_i1-pad1_1k
r5 net-_r5-pad1_net-_q13-pad2_2k
r2 net-_q5-pad1_net-_i1-pad1_1k
r4 net-_q6-pad2_net-_r4-pad2_250
* u1 net-_i1-pad1_net-_q10-pad3_net-_c1-pad2_net-_q2-pad1_net-_q5-pad1_net-_r5-pad1_net-
_r4-pad2_port
.tran 0e-00 0e-00 0e-00

```

* Control Statements

```

.control
run
print allv > plot_data_v.txt
print alli > plot_data_i.txt

```

* /home/ashwini/esim-workspace/uc1525osc1/uc1525osc1.cir

```

.include ucosc.sub
x1 net-_x1-pad1_net-_x1-pad2_net-_r2-pad2_net-_r1-pad2_outr net-_x1-pad2_outt ucosc
v1 net-_x1-pad2_gnd_dc 12
v2 gnd net-_x1-pad1_dc 12
r1 gnd net-_r1-pad2_7k
r2 outr net-_r2-pad2_10k
c1 outr gnd 0.05u
* u2 outt plot_v1
* u1 outr plot_v1
.tran 0.1e-06 4e-03 0e-00

```

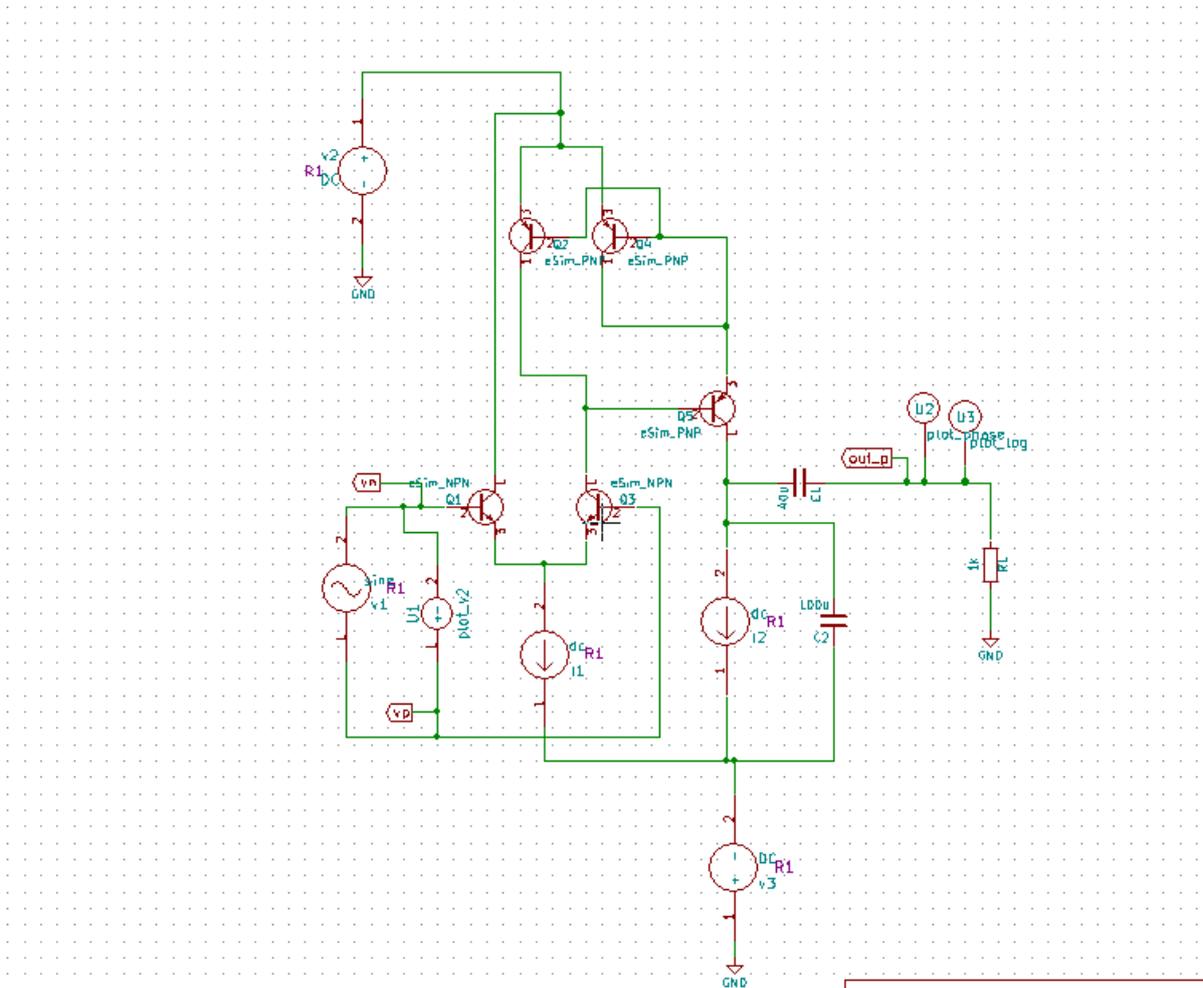
* Control Statements

```

.control
run
print allv > plot_data_v.txt
print alli > plot_data_i.txt
plot v(outt)
plot v(outr)
.endc
.end
.endc
.end

```

UC1525 subcircuit error amplifier:



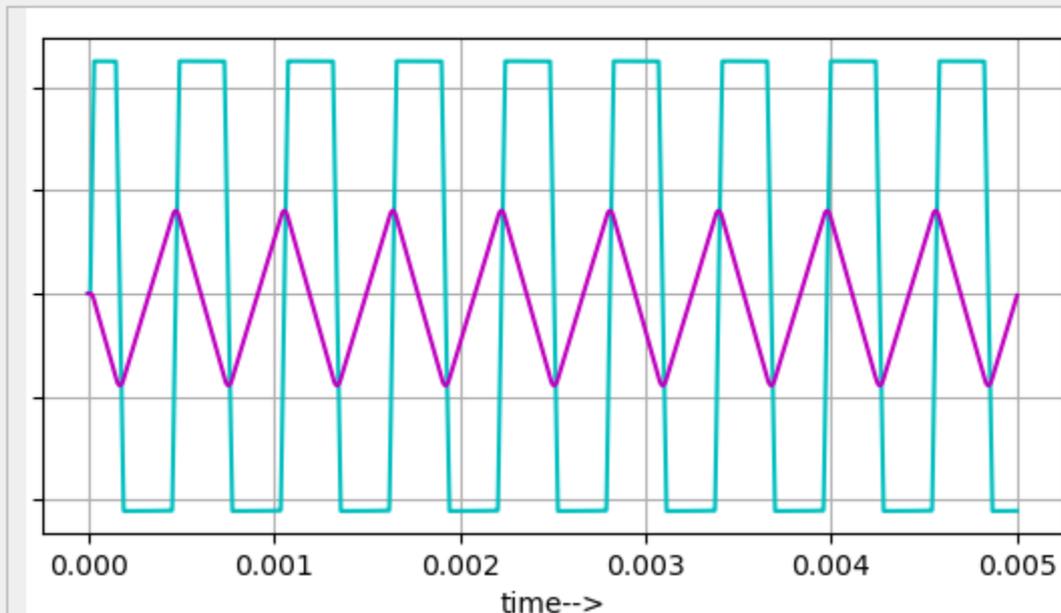
Netlist generated from eSim:

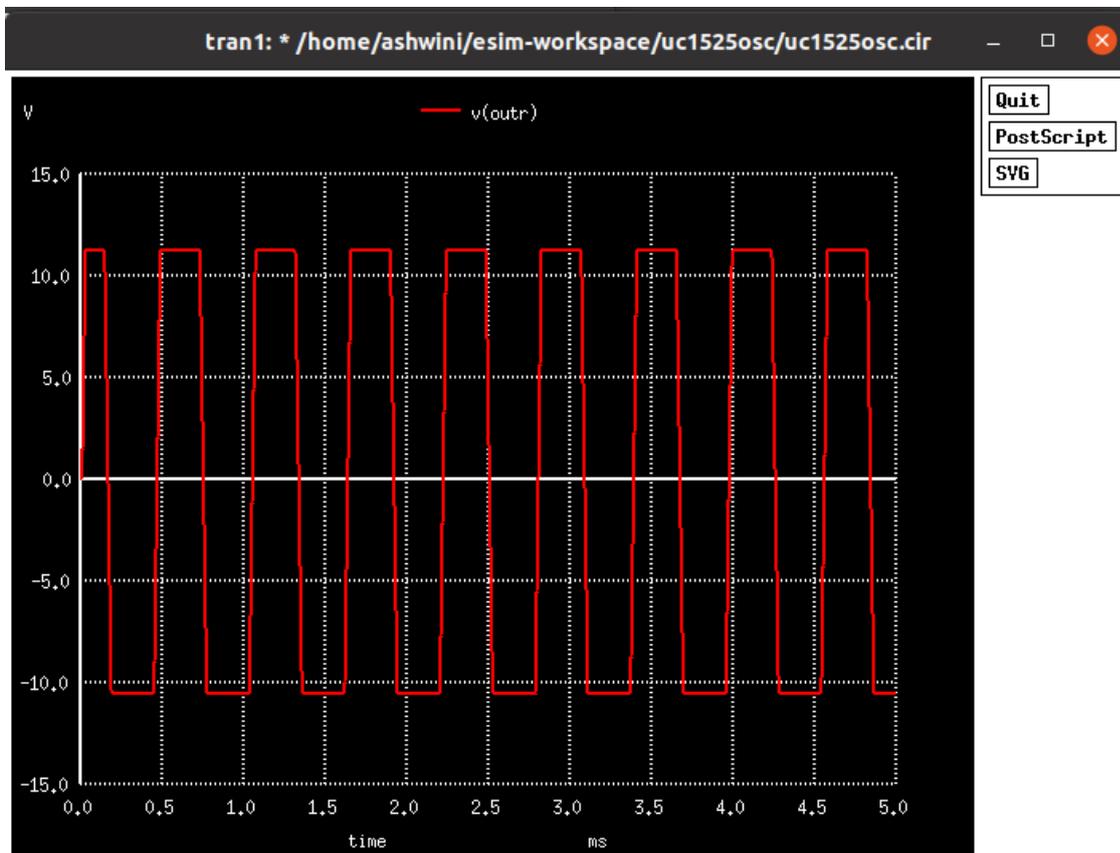
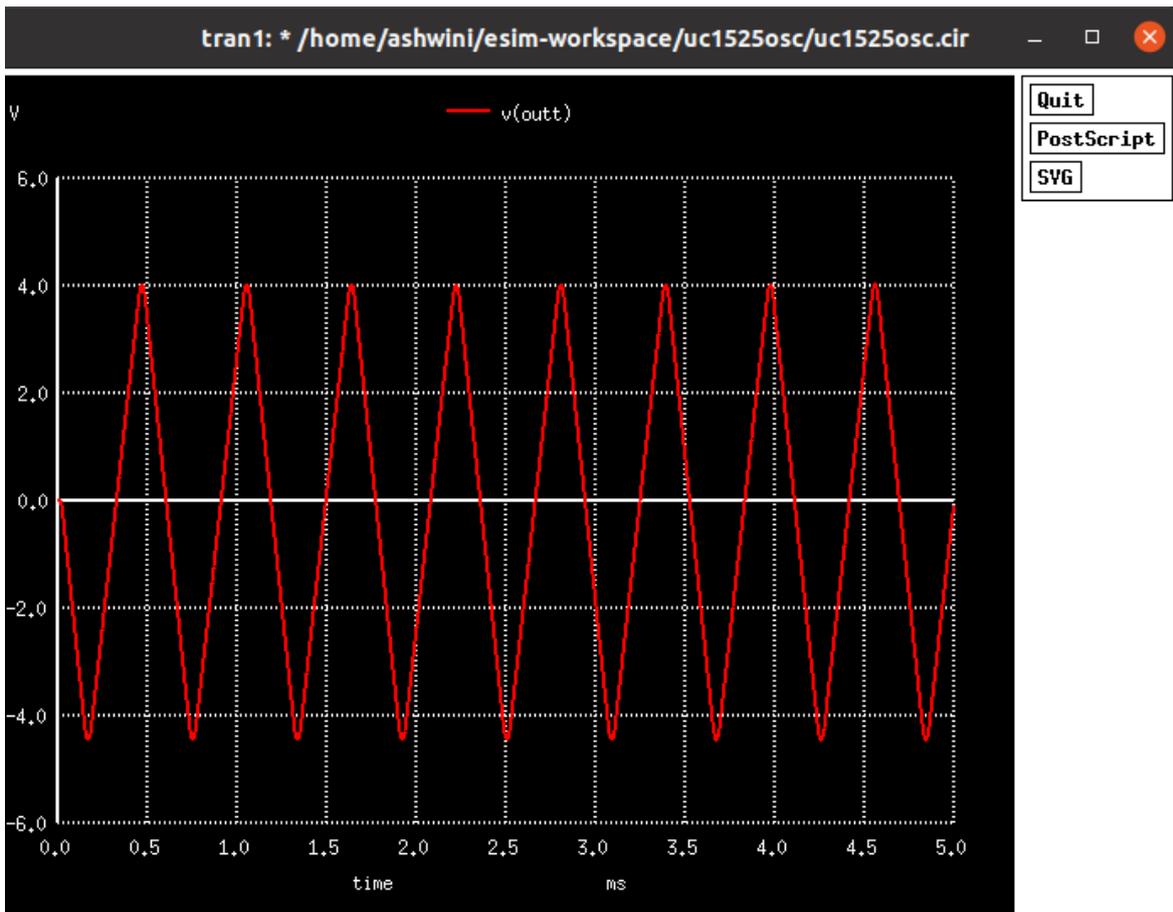
```
*/home/ashwini/eSim-Workspace/uc1525_error_amplifier/  
uc1525_error_amplifier.cir  
  
* EESchema Netlist Version 1.1 (Spice format) creation date: Mon May 13 14:29:53  
2024  
  
* To exclude a component from the Spice Netlist add [Spice_Netlist_Enabled] user  
FIELD set to: N  
* To reorder the component spice node sequence add [Spice_Node_Sequence]  
user FIELD and define sequence: 2,1,0  
  
* Sheet Name: /  
Q3 Net-_Q2-Pad1_Net-_Q3-Pad2_Net-_Q1-Pad1_eSim_PNP  
Q4 Net-_Q3-Pad2_Net-_Q3-Pad2_Net-_Q1-Pad1_eSim_PNP  
Q1 Net-_Q1-Pad1_Net-_Q1-Pad2_Net-_I1-Pad2_eSim_NPN  
Q2 Net-_Q2-Pad1_Net-_Q2-Pad2_Net-_I1-Pad2_eSim_NPN  
Q5 Net-_C1-Pad2_Net-_Q2-Pad1_Net-_Q3-Pad2_eSim_PNP  
I1 GND Net-_I1-Pad2_dc  
I2 GND Net-_C1-Pad2_dc  
U1 GND Net-_C1-Pad2_zener  
v2 Net-_Q1-Pad1_GND DC  
v1 Net-_Q2-Pad2_Net-_Q1-Pad2_sine  
R1 out GND 100k  
C1 out Net-_C1-Pad2_100u  
  
.end
```

Result:

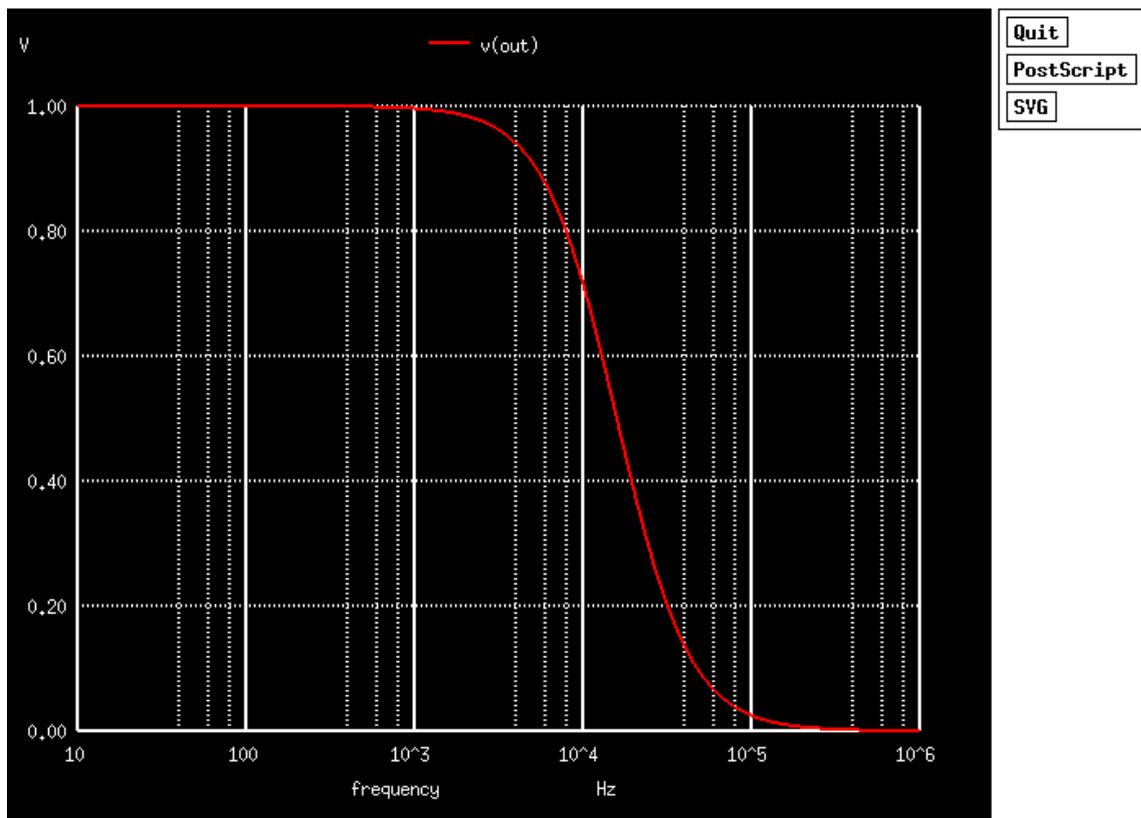
UC1525B Oscillaor circuit result screen-shot

Plotting-2





UC1525B error amplifier bode plot



References:

[1] SWITCHED MODEL OF CONTROL CIRCUITS-FOR DC-DC SWITCHING CONVERTERS: APPLICATION TO INTEGRATED CIRCUITS UC1525 AND UC1846. Alfonso Lago, Carlos M. Pefialver, Jeslis Cea. Dpto. Tecnologia Electrónica. E.T.S.I.I. Universidad de Vigo. Lagoas-Marcosende,g. Apartado Oficial. 36200-VIGOSPAIN.

[2] esim.fossee.in > [circuit-simulation-project](https://esim.fossee.in/circuit-simulation-project)To study of High & Low frequency response of FET - esim.fossee.in

[3] <https://github.com/FOSSEE/eSim>