

SWITCHED MODEL OF CONTROL CIRCUITS FOR DC-DC SWITCHING CONVERTERS: APPLICATION TO INTEGRATED CIRCUITS UC1525 AND UC1846.

Alfonso Lago, Carlos M. Peñalver, Jesús Cea.

Dpto. Tecnología Electrónica. E.T.S.I.I. Universidad de Vigo.
Lagoas-Marcosende,9. Apartado Oficial. 36200-VIGO-SPAIN.

ABSTRACT:

Two modelation techniques are the most usual today: the average model, which is very conventional, where voltages and/or currents are applied continuously in a scaling form, and the switched model, where voltages and/or currents are applied for a short fraction of the conmutation period.

In this paper the switched model technique and the simulation of control PWM circuits for switch mode DC/DC power converters are described. This model has been developed using Intusoft ISSPICE/286 software, which is based on SPICE2G.6 from University of Berkeley. Spice simulation is a halfway step between circuit theoretic design and its practical implementation and it allows to reduce design time and to observe and to correct some unwanted or unpredictable features of the theoretic design.

The modelation and simulation techniques are applied to the popular control PWM integrated circuits UC1525 and UC1846. Several parts, which are simulated together with subcircuits list, like the oscillator, the error amplifier and the comparator, are described. Finally, the efficacy of this model is verified.

1. INTRODUCTION.

The most widespread modelation

technique used today is the average model, which is very conventional, where voltages and/or currents are applied continuously in a scaling form. An important aspect to consider about the average model is that high frequencies phenomena, due to the conmutation process, are not considered. It is therefore necessary to build new, more complex, models that take into account these phenomena. This is an important aspect to consider in the selection of a suitable model for the modelation.

Different solutions to improve the average model technique have been achieved. Some of them adjust different defects and extend the range of application, but they produce artificial and abstract models which make results misunderstand and difficult.

In this paper the switched model technique and the simulation of control PWM circuits for switch mode DC/DC power converters are described. In the switched model, voltages and/or currents are applied for a short fraction of the conmutation period, allowing to consider several phenomena (that they are hidden from the average model) to simulate them, but the simulation time is very long. This model has been development using Intusoft ISSPICE/286 software, which is based on SPICE2G.6 from University of Berkeley.

Spice simulation is a halfway step between circuit theoretic design and its

practical implement and it allows to reduce design time and to observe and correct some unwanted and unpredictable features of the theoretic design.

In this paper, this modelation and simulation technique is applied to popular control PWM integrated circuits UC1525 and UC1846. Several parts are described and simulated together with subcircuits lists, including oscillator, error amplifier and comparator. Finally, the efficacy of this model is verified.

2. SWITCHED MODEL.

In the switched model, the voltages and/or currents are applied to the circuit during each switching period, the appropriate fraction of time producing a simplified version of the circuit. A proper switched model will produce results wich are easily interpreted [DIXO 91].

This model works with square waveforms and the step time from high level to low level and vice versa force to very long simulation times. Therefore many iterations during each switching period are needed.

This problem can be solved if initial conditions are set close to the expected final values. So, short run times of only a few cycles can evaluate most switching related effects and therefore reduce the simulation final time.

Other topic is the convergence in the analysis, especially in the case if small internal timesteps in transient analysis. This can be avoided by forcing the switches of the circuit to be closed/opened to perform the initial conditions.

Subjects appropriate for switched

model include:

- High frequencies phenomena.
- Check high frequency closed loop stability.
- Evaluate converter performance in the start.
- Check effects of leakage and wiring inductance on load regulation. Evaluate transformer design factors for improvement.
- Evaluate effects of transistor switching speed and rectifier recovery.
- Observe resonant power converter operation over the switching cycle.
- Evaluate circuits where theory is inadequate, such as closed loop performance of resonant power converters, especially with variable frequency operation, etc.

3. SWITCHED MODEL OF CONTROL CIRCUIT UC1525.

The simulation of UC1525 circuit does not cover all possibilities of the real circuit because some of the characteristics have not been considered important from simulation point of view. Other features have been modified according to the simulation software. The most important differences are:

- The circuit starts with inital conditions. Therefore, soft start and shutdown are not needed.
- The synchronism input has been eliminated because it causes many convergence problems and it is not essential.
- The circuit outputs have been simulated through a voltage-controlled voltage source. When the switches of actual circuit are closed the source voltage is 1V and when they are opened the voltage is 0V. Therefore, it is not

necessary to power on the circuit (input V_C in the real circuit).

In addition, the UC1525 has been simulated with both one and two outputs. The simulation time with ISSPICE/286 is very long and it is recommended to use the version with two outputs only in circuits with several switching transistors.

This paper studies the version with one output. Figure 1 illustrate the UC1525 circuit with its net list.

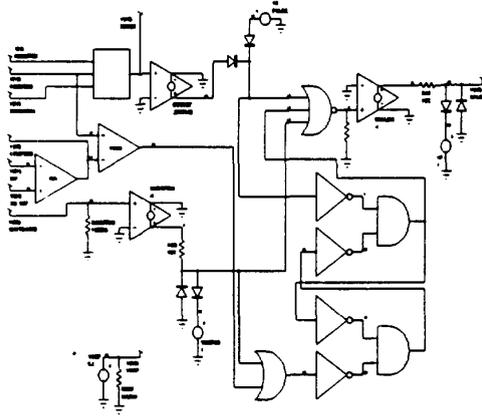


Figure 1: Switched model of integrated circuit UC1525 with one output.

```
.SUBCKT UC1525_1 32 24 31 22 19 33 4 10 38 15
* 32-> Shutdown
* 24-> Ninv
* 31-> Inv
* 22-> Compensación
* 19-> Ct
* 33-> Descarga
* 4-> Rt
* 10-> Osc out
* 38-> Salida
* 15-> Vref
.MODEL DIODO D(N=1M RS=1M)
X3 22 19 23 PWM25
RSHUTDOWN 32 0 10MEG
X5 35 20 30 5 NOR3
```

```
VREF 15 0 5.1
RREF 15 0 10MEG
R5 5 0 1MEG
ERESSET 34 0 10 0 .2857142
E2SHUTDOWN 2 0 32 0 -8 10
RSD 2 30 10K
D4 0 30 DIODO
D5 30 11 DIODO
VREFSD 11 0 1
X10 35 9 INV
X11 29 28 INV
X12 26 25 INV
X13 20 27 INV
X14 9 25 20 AND2
X15 27 28 26 AND2
X16 30 23 29 OR2
X17 31 24 22 ERRAMP25
D6 34 35 DIODO
D7 16 35 DIODO
V8 16 0 PULSE 1 0
ESALIDA 37 0 5 0 -8 10
R10 37 38 10K
D8 38 39 DIODO
V9 39 0 1
D9 0 38 DIODO
X1 19 4 33 10 OSC25
.ENDS
```

Simplified model of the control circuit UC1525 with one output.

Error Amplifier: The error amplifier is a transconductance amplifier with a DC gain in open loop of 75dB (subcircuit ERRAMP25)).

The input impedance is modeled by capacitor CERR_INP and resistor RERR_INP. Voltage source EOFFSET simulate the offset voltage. Voltage-controlled current source GERR_AMP and resistor RERR_OUT give the open-loop gain. Capacitor CERR_OUT gives the bandwidth of the error amplifier. Finally, D1, D2, VERR_MIN and VERR_MAX limit the amplifier output voltage between 0.2 and 5.6V.

```
.SUBCKT ERRAMP25 16 19 4
* 16-> Ninv
* 19-> Inv
* 4-> Compensación
```

```

RERR_INP 16 19 100K
CERR_INP 16 19 1P
GERR_AMP 0 4 19 3 1.5M
RERR_OUT 4 0 3.75MEG
CERR_OUT 4 0 119.345P
D1 5 4 DIODO
VERR_MIN 5 0 .2
D2 4 6 DIODO
VERR_MAX 6 0 5.6
R2 3 0 1MEG
EOFFSET 3 0 16 0 2M 1
.ENDS

```

Oscillator: The UC1525 oscillator defines the switching frequency of the system. A resistor and a capacitor are externally connected. A second resistor between the capacitor and the discharge terminal provides a wide range of dead-time adjustment. Oscillator frequency is approximately defined by:

$$f = \frac{1}{C_t * (0.7R_t + 3R_d)}$$

The oscillator is modeled based on comparator LM111 and voltage-controlled voltage source EGENREF.

```

.SUBCKT OSC25 12 5 33 41
* 12->Ct
* 5->Rt
* 33->Descarga
* 41->Osc out
FSEGUIDR 0 12 VTEST_1 1
VTEST_1 13 5 0
XCOMP 45 8 4 0 39 0 LM111
VALIMEN+ 39 0 10
ESEGUID- 8 0 0 12 -1
EGENREF 45 0 4 0 0.6240756 0.5751848
EC_CARGA 0 1 0 45 5 1.4285714
QDESC_1 33 11 0 Q2N2923
QDESC_2 33 29 11 Q2N2923
RDESC 11 0 1K
EDESC 29 0 0 45 1.6875 .4821428
VCOMP 10 0 5
ESALIDA 41 0 45 0 4.375 -1.25
RSALIDA 41 0 1MEG
R4 4 10 1K
VREFOSC 13 1 PULSE 0 4
.ENDS

```

Comparator: This circuit compares the output of the error amplifier with the capacitor voltage to obtain the control signal of the DC-DC converter. Initially, both voltages are limited between 0.9-3.3V. Subsequently, they are subtracted and the result is multiplied by 1000 (60dB). Finally, the output is limited between 0-1V. If the capacitor voltage is below the amplifier output, the comparator output is 0V, otherwise is 1V.

```

.SUBCKT PWM25 14 15 8
* 14->Inv
* 15->Ninv
* 8->Salida PWM
VREF1 1 0 0.9
RREF1 6 12 10K
D2 6 3 DIODO
VREF2 3 0 3.3
D7 4 2 DIODO
VREF3 4 0 0.9
RREF2 2 13 10K
D8 2 7 DIODO
VREF4 7 0 3.3
EPWM 10 0 6 2 1K
D9 0 8 DIODO
RPWMOUT 8 10 10K
D10 8 11 DIODO
VPWMOUT 11 0 1
ESEG1 12 0 15 0 1
ESEG2 13 0 14 0 1
D1 1 6 DIODO
.ENDS

```

4. SWITCHED MODEL OF CONTROL CIRCUIT UC1846.

Current-mode control effectively eliminates the phase lag of control function, associated with the output filter inductor or the energy-storage inductor. The current-mode controllers developed differ slightly in their phase-lag characteristics.

All types of current-mode controllers command directly the current in the inductor of the power converter. Hence, the inductor current follows instantaneously the control

input.

This paper considers the operation mode in which the inductor current is compared with the control signal (in the case of voltage regulated converters, the error amplifier output) and the decision making comparator turns off the power switch when the increasing inductor current reaches the value commanded by the control signal. The power switch is turned "on" again when the inductor current decreases by a chosen amount, I .

The most important differences of the simulation of this circuit with respect to real circuit are the same that the simulation of UC1525.

The UC1846 has been simulated with both one and two outputs but it is recommended to use the version with two outputs only in circuits with several switching transistors.

This paper studies the version with one output. Figure 2 illustrates the UC1846 circuit with its netlist.

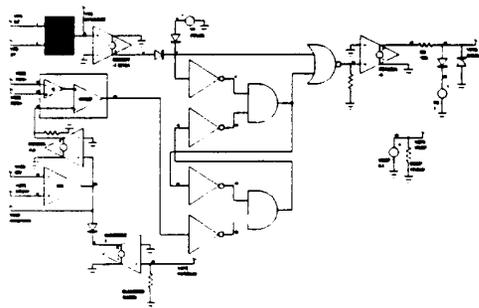


Figure 2: Switched model of integrated circuit UC1846 with one output.

```
.SUBCKT UC1846_1 26 27 19 29 30 2 1 3 21 18 31
* 26->Compensación
```

```
* 27->Ninv
* 19->Inv
* 29->Curr sense (-)
* 30->Curr sense (+)
* 2->Ct
* 1->Rt
* 3->Sync out
* 21->Vref
* 18->Salida
* 31->Currlim
.MODEL DIODO D(N=1M RS=1M)
X2 23 29 30 15 COMP46
ERESET 6 0 3 0 -1.12194 .4878
D1 6 7 DIODO
D2 8 7 DIODO
V1 8 0 PULSE 1 0
X4 7 9 INV
X5 14 11 INV
X6 13 10 INV
X7 15 12 INV
X8 9 10 14 AND2
X9 11 12 13 AND2
X11 7 14 16 NOR2
R1 16 0 1MEG
ESALIDA 17 0 16 0 -8 10
R2 17 18 10K
D3 18 20 DIODO
V2 20 0 1
D4 0 18 DIODO
VREF 21 0 5.1
RREF 21 0 10MEG
X12 27 19 26 ERRAMP46
ERESTA 23 0 26 0 -0.5 1
R5 23 0 1MEG
ELIMCURR 5 0 31 0 1
D5 26 5 DIODO
RLIMCURR 31 0 10MEG
X1 2 1 3 OSC46
.ENDS
```

Simplified model of the control circuit UC1846 with one output.

Error Amplifier. The error amplifier is a transconductance amplifier with a DC gain in open loop of 105dB (subcircuit ERRAMP46)).

The input impedance is modeled by capacitor CERR_INP and resistor RERR_INP. Voltage source EOFFSET simulate the offset voltage. Voltage-

controlled current source GERR_AMP and resistor RERR_OUT give the open-loop gain. Capacitor CERR_OUT gives the bandwidth of the error amplifier. Finally, D1, D2, VERR_MIN and VERR_MAX limit the amplifier output voltage between 0.7 and 4.6V.

```
.SUBCKT ERRAMP46 6 8 4
* 6->Ninv
* 8->Inv
* 4->Compensación
EOFFSET 3 0 8 0 .5M 1
GERR_AMP 0 4 6 3 4.1121
RERR_OUT 4 0 43246
R2 3 0 1MEG
CERR_OUT 4 0 .6544465U
CERR_INP 8 6 1P
D1 4 5 DIODO
VERR_MAX 5 0 4.6
D2 7 4 DIODO
VERR_MIN 7 0 .7
RERR_INP 8 6 100K
.ENDS
```

Oscillator. The UC1846 oscillator defines the switching frequency of the circuit through a resistor and a capacitor externally connected. Oscillator frequency is approximately determined by:

$$f = \frac{2200}{C_t * R_t} \quad (R_t > 10K)$$

where $R_t = [k]$ and $C_t = [\mu F]$.

Discharge time is determined by:

$$\tau_d = 145 * C_t$$

The oscillator model is based on comparator LM111 and voltage-controlled voltage source EGENREF.

The voltage source VREFOSC has been defined "PULSE" to eliminate DC

convergence errors.

```
.SUBCKT OSC46 12 5 43
* 12->Ct
* 5->Rt
* 43->Sync out
FSEGUIDR 0 12 VTEST_I 1
VTEST_I 13 5 0
XCOMP 45 8 4 0 39 0 LM111
VALIMEN+ 39 0 10
ESEGUID- 8 0 0 12 -1
EC_CARGA 0 1 0 45 7.3580645 3.2258065
VCOMP 10 0 5
ESALIDA 43 0 45 0 5.2576534 -1.2966477
RSALIDA 43 0 1MEG
R4 4 10 1K
EGENREF 45 0 4 0 .6571298 .324774
GDESC 12 0 45 0 .017313 -7.5901328M
VREFOSC 13 1 PULSE 0 5.1
.ENDS
```

Comparator. Initially, the difference between current sense inputs is multiplied by 3 (9,5dB). This voltage is compared with the error amplifier output. The result is amplified by 1000 (60 dB) and limited to 0 - 1V range through diodes and auxiliary sources.

```
.SUBCKT COMP46 11 3 1 14
* 11->Entrada inversora
* 3->Curr sense (+)
* 1->Curr sense (-)
* 14->Salida del comparador
ECMP_AMP 4 0 3 1 -15M 3
D1 8 2 DIODO
VLIM+ 2 0 3.6
ECOMPAMP 6 0 8 11 1000
D3 0 14 DIODO
D4 14 9 DIODO
VCMP_OUT 9 0 1
RREF1 4 8 10K
RREF2 6 14 10K
RCMP_ENT 1 3 10MEG
.ENDS
```

Current Limit Adjust Section. The current limit adjust input is modeled by diode D5, resistor RLIMCURRE and voltage-controlled voltage source ELIMCURRE (netlist UC1846_1). This input permits a

pulse-by-pulse current limiting.

If R is the current sense resistor, the maximum current is determined by the formula:

$$I = \frac{V - 0,5}{3R}$$

where:

- V = Current Limit Input Voltage.
- 0,5 = Current Limit Offset Voltage.

5. EXPERIMENTAL RESULTS.

Figure 3 shows the open-loop voltage gain and phase of the UC1525 error amplifier. That gain has been simulated for two values of the impedance from output pin to ground. Values below 30K will begin to limit the maximum duty cycle.

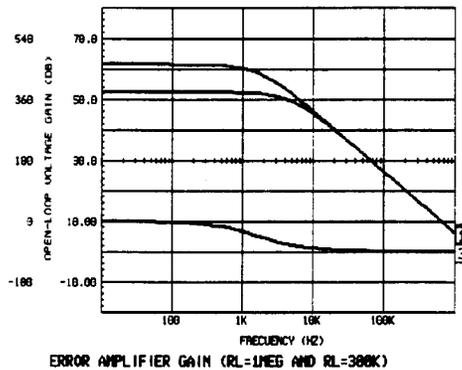


Figure 3: Error Amplifier Gain and Phase vs Frequency.

Figure 4 shows the UC1525 oscillator ramp signal. The ramp valley is 0.9V and the ramp peak is 3.3V.

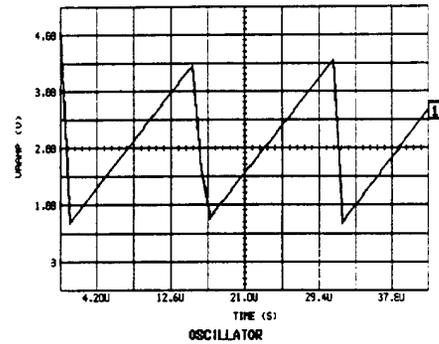


Figure 4: Oscillator ramp signal.

Figure 5 shows the PWM control signal (waveform 3) limited between 0-1V. The rise times and fall times of this signal are improved through the output stage.

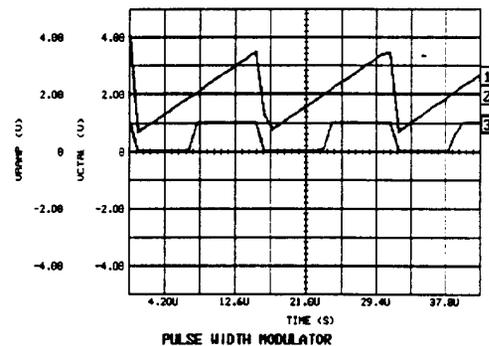


Figure 5: PWM Control Signal.

Figure 6 shows the open-loop voltage gain of the UC1846 amplifier error. That gain has been simulated for an impedance from output pin to ground of 10K. Figure 7 shows the oscillator ramp signal and the sync signal. The ramp valley is 1V and the ramp peak is 2.25V.

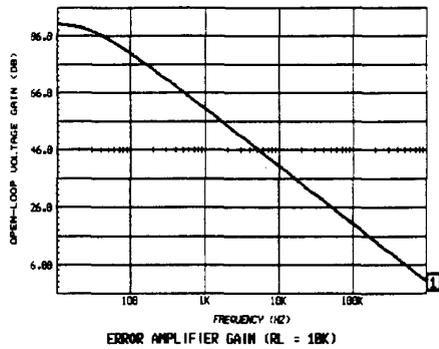


Figure 6: Error Amplifier Gain vs Frequency.

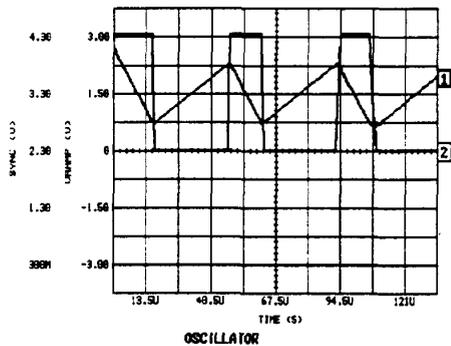


Figure 7: Oscillator ramp and sync signal

6. CONCLUSIONS.

A switched model technique is described in this work. Advantages and appropriate subjects for switched model are indicated, where voltages and currents are applied for a short time of the conmutation period for to be able to simulate hidden phenomena from the average model.

This model and its simulation is applied to control integrated control circuits UC1525 and UC1846. The more significative

blocks of this circuit, like oscillator, error amplifier and comparator, are simulated and studied.

7. REFERENCES.

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