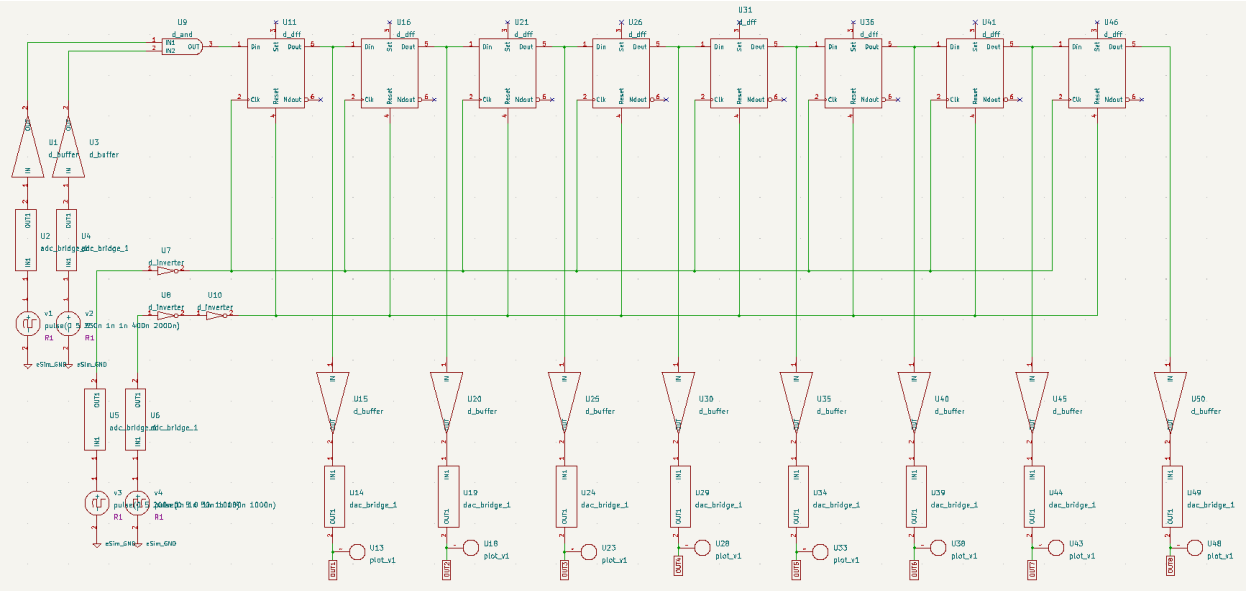
Title of the circuit : 8 Bit Serial-In Parallel-Out Shift Register using D Flip-Flops

Theory/Description :

The given circuit is an 8-bit Serial-In Parallel-Out (SIPO) shift register designed using cascaded flip-flops to convert serial data into parallel output. The circuit consists of eight D flip-flops connected in series, where the output of each flip-flop serves as the input to the next stage. Serial data is applied to the first flip-flop, and with each clock pulse, the data is shifted sequentially through the register stages. A common clock signal synchronizes all flip-flops, ensuring controlled and timed data transfer across the system. The reset or clear input initializes all flip-flops to a known state, typically zero, before operation. As data shifts through the register, each stage stores one bit, enabling simultaneous access to all stored bits through parallel outputs (Q0 to Q7). This architecture effectively converts serial input data streams into parallel form, improving data handling efficiency in digital systems. The SIPO shift register is widely used in communication systems, data storage, and interfacing applications where serial-to-parallel conversion is required. It provides a simple and efficient method for expanding input/output capabilities in microprocessor and digital logic systems.

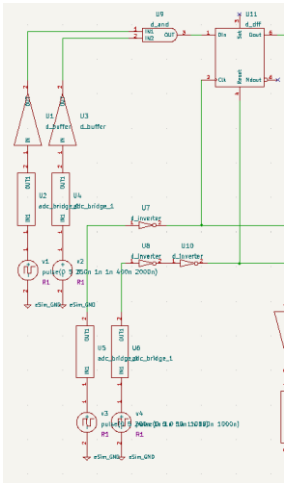


8 Bit Serial-In Parallel-Out Shift Register Circuit

8-BIT SIPO SHIFT REGISTER CIRCUIT

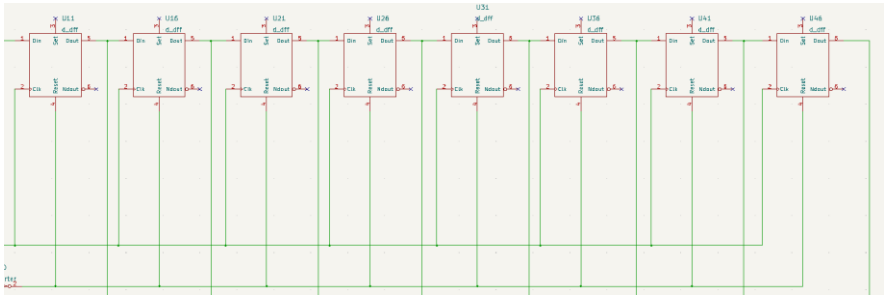
Stage 1: Serial Input and First Flip-Flop Stage

The first stage of the circuit consists of the initial D flip-flop which receives the serial input data. The input data stream is applied to the D input of the first flip-flop. A clock signal controls when the data is sampled and stored. On every clock pulse, the input bit is latched into the first flip-flop. This stage acts as the entry point for the entire register. It ensures proper synchronization between input data and the clock signal. The accuracy of this stage is critical for correct data shifting. It initiates the serial-to-parallel conversion process.



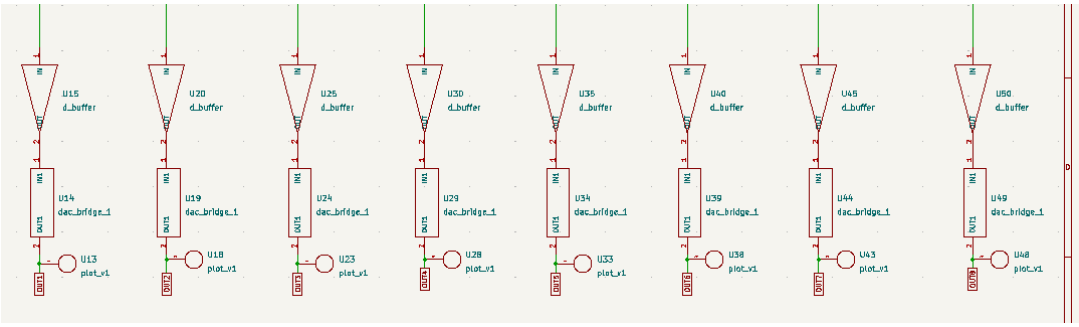
Stage 2: Cascaded Shift Register Stages (Data Propagation Stage)

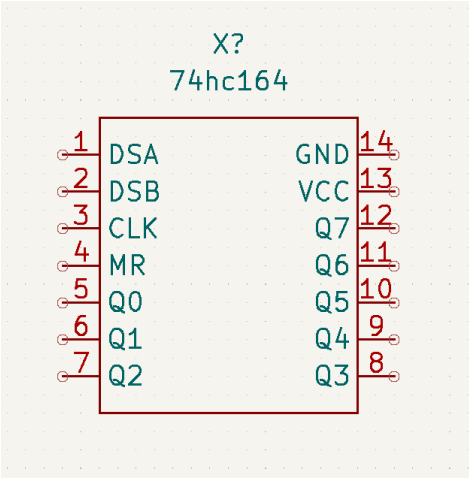
The second stage consists of multiple D flip-flops connected in cascade (from FF2 to FF8). The output (Q) of each flip-flop is connected to the input (D) of the next flip-flop. With each clock pulse, the stored data shifts one position to the right. This creates a sequential movement of bits across the register. Each flip-flop stores one bit of data at a time. After 8 clock pulses, the complete 8-bit data is distributed across all stages. This stage enables temporary data storage and controlled data movement. It forms the core shifting mechanism of the SIPO register.



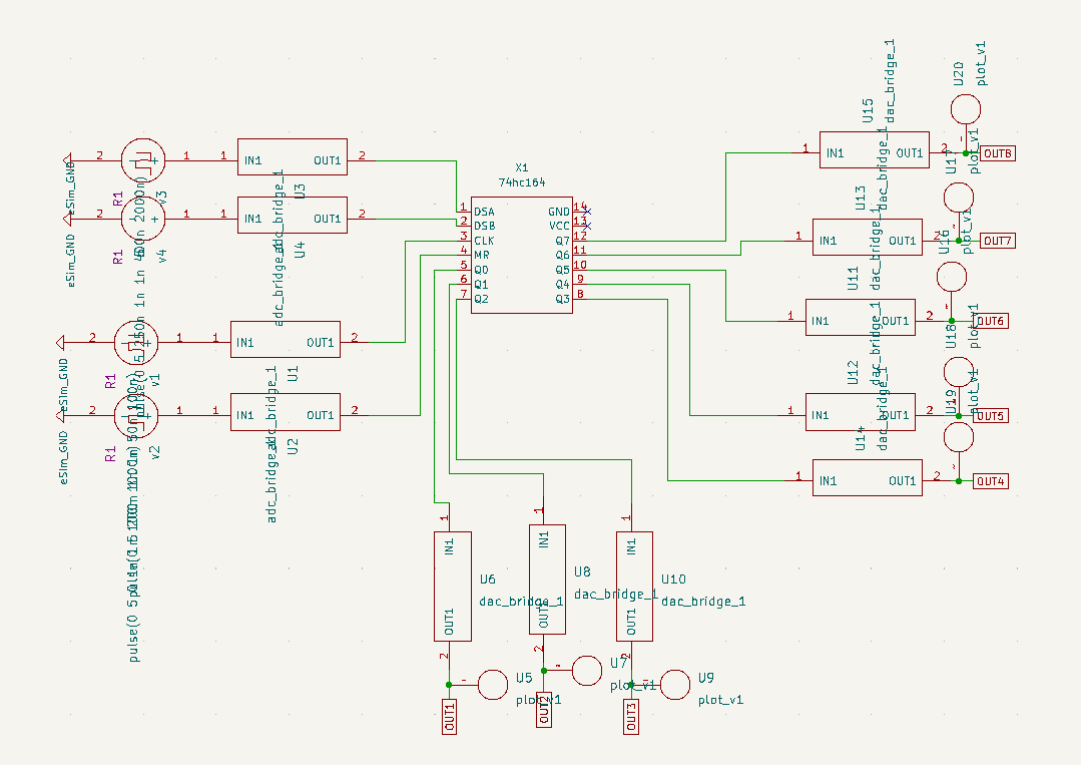
Stage 3: Parallel Output and Control Stage

The final stage provides parallel outputs from all flip-flops (Q0 to Q7). Each flip-flop output represents one bit of the stored data. All outputs can be accessed simultaneously after the shifting operation is complete. A reset/clear input is used to initialize all outputs to zero before operation. This ensures predictable and error-free system behavior. The parallel outputs allow easy interfacing with other digital circuits. This stage completes the serial-to-parallel data conversion process. It determines the usability of the register in real-time applications.





SUB CIRCUIT SYMBOL OF AD797



TEST CIRCUIT

Signal Characteristics

Input Signal Characteristics

1. Signal Type

The inputs are digital pulse signals used to control data shifting and register operation.
They represent binary logic levels (0 V for LOW and 5 V for HIGH).

2. DC Levels

The logic LOW level is 0 V and the logic HIGH level is 5 V.
These voltage levels ensure proper operation of digital flip-flops in the circuit.

3. Serial Data Input (DSA)

The DSA input is a pulse signal representing the serial data stream.
It starts at 250 ns and alternates between HIGH and LOW states.
The pulse width is 400 ns with a total period of 2000 ns.
This defines the rate at which data bits are fed into the register.

4. Secondary Data Input (DSB)

The DSB input is maintained at a constant HIGH level of 5 V.
This ensures a fixed logic input condition for the circuit configuration.
It can act as a control or enable input depending on the design.

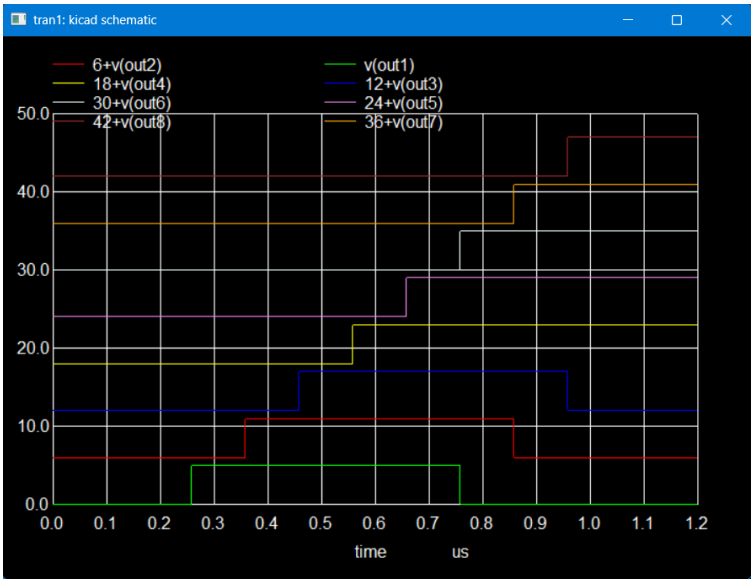
5. Clock Signal (CLK)

The clock signal is a periodic pulse that controls data shifting.

It has a pulse width of 50 ns and a period of 100 ns.
Each rising edge of the clock triggers data transfer between flip-flops.
This determines the speed of operation of the shift register.

6. Master Reset (MR)

The MR signal is used to initialize the register.
It starts at 0 ns and produces a HIGH pulse for 100 ns.
When activated, it clears all flip-flops and sets outputs to zero.
This ensures proper starting conditions before data shifting begins.



Test Circuit Output

Detailed Characteristics Analysis of Output Signal

1. Timing and Synchronization

The most critical characteristic of a SIPO register is the relationship between the clock and the data movement.

- Shift Interval (): The signals show a precise shift interval of 0.1 s between successive stages (e.g., from out1 to out2).
- Operating Frequency (): Since the shift occurs every 0.1 s, the simulation reflects a clock frequency of:
- Cumulative Latency: To reach the final stage (out8), the data requires 7 clock cycles of delay from the first stage. Total latency from input to the 8th bit is approximately 0.7 s.

2. Pulse Width and Duty Cycle

- Pulse Duration (): The high-state duration for each output is 0.5 s. This indicates that the serial input data string was a sequence of five logic "1"s (since).
- Symmetry: The pulse width is maintained perfectly across all stages, showing that there is no pulse-width distortion or "jitter" in this simulation environment.

3. Signal Amplitude and Offsets

- Logic High (): The actual logic high appears to be 5V (standard TTL/CMOS level).
- DC Offsets: To distinguish the 8 bits, constant DC offsets were added in the plotting expression:
    - out1: 0V base
    - out2: 6V base ()
    - out3: 12V base ()
    - *Pattern:* Each stage is offset by an additional 6V to prevent overlap.

4. Transition Characteristics

- Rise/Fall Time (): In this specific simulation, the transitions appear near-instantaneous (ideal). In a real-world CMOS implementation (like a 74HC594), you would see a slight slope and potential ringing.
- Propagation Delay (): The data shifts exactly on the trigger point. In physical hardware, there would be a nanosecond-scale delay between the clock edge and the output transition.

5. State Retention

- **End-of-Simulation Status:**
    - Stages out1 through out3 have successfully returned to Logic 0, meaning the 5-bit high pulse has completely passed through them.
    - Stages out4 through out8 are still Logic 1 at the 1.2 s mark. This indicates the register is "holding" the bits. If the simulation continued for another 0.5 s, these would also drop to zero.

Source/Reference(s) :

1. 74HC164BQ Datasheet, *NXP Semiconductors*
   - Primary reference for internal logic structure, timing characteristics, and functional operation of the shift register.
2. M. Morris Mano, Digital Design, *Pearson Education*
   - Explains fundamental concepts of shift registers, sequential circuits, and serial-to-parallel data conversion.