Implementation of a Sinc3 Digital Decimation Filter using eSim and HDL

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***Abstract*—This paper presents the research migration of a Sinc3 digital decimation filter into the eSim open-source EDA environment. The Sinc3 filter is a vital component in Sigma-Delta Analog-to-Digital Converters (ADCs), serving as the primary stage for noise suppression and sample rate reduction. By utilizing eSim's mixed-signal simulation capabilities—integrating Ngspice for analog transients and GHDL for hardware description language (HDL) logic—this study successfully reproduces validated research results in an open-source framework.**

***Index Terms*—eSim, Sinc3 Filter, CIC Filter, Decimation, GHDL, Ngspice, FOSSEE, Open-Source EDA.**

I. Introduction

The FOSSEE project at IIT Bombay promotes the "Research Migration Project" to bridge the gap between proprietary and open-source EDA tools. Digital Signal Processing (DSP) often relies on proprietary tools like MATLAB for architectural validation.

The Sinc3 filter, or third-order Cascaded Integrator-Comb (CIC) filter, is the architecture of choice for high-speed decimation due to its multiplier-free hardware realization. This report documents the systematic migration of this circuit to eSim, ensuring that the results are consistent with standard IEEE research benchmarks.

II. Theoretical Background

A. The Sinc3 Transfer Function

The Sinc3 filter provides high attenuation at folding frequencies. In the z-domain, the transfer function of a single-stage CIC filter is:

$$H(z) = \sum_{k=0}^{N-1} z^{-k} = \frac{1 - z^{-N}}{1 - z^{-1}} \tag{1}$$

For a Sinc3 filter, three such stages are cascaded:

$$H(z) = \left(\frac{1 - z^{-N}}{1 - z^{-1}} \right)^3 \tag{2}$$

where N is the decimation ratio.

B. Bit-Growth and Register Width

A critical challenge in Sinc3 design is register overflow. Since the integrators do not have a reset, the registers must be wide enough to wrap around without losing data integrity. The required bit-width (W) for an M-stage Sinc filter with an input width B_{in} is:

$$W = B_{in} + M \log_2(N) \tag{3}$$

For $N = 64$ and $M = 3$, the bit growth is 18 bits beyond the input.

III. System Architecture

The system architecture follows the Hogenauer structure, divided into high-rate and low-rate processing zones.

A. Integrator Section

Operating at the high sampling rate (f_s), these stages accumulate the input bitstream. In eSim, these are implemented as Verilog always blocks.

B. Decimation and Comb Section

The decimator reduces the rate by N. The comb section then calculates the difference between the current and previous decimated samples:

$$y[n] = x[n] - x[n - k] \tag{4}$$

where k is the differential delay (usually $k = 1$).

IV. eSim Implementation Methodology

A. Digital Logic Development (GHDL)

The digital part of the filter is modeled in Verilog. This allows eSim to use GHDL for logic verification while Ngspice handles the analog interface.

```
always @(posedge clk_high) begin
    // Integrator Stages
    i1 <= i1 + din;
    i2 <= i2 + i1;
    i3 <= i3 + i2;
end

always @(posedge clk_low) begin
    // Comb Stages
    c1 <= i3 - i3_z1;
    c2 <= c1 - c1_z1;
    c3 <= c2 - c2_z1;
    // Delay Updates
    i3_z1 <= i3;
    c1_z1 <= c1;
    c2_z1 <= c2;
```

```
end
```

Listing 1. Verilog Implementation of Sinc3 Stages

B. Mixed-Signal Integration

In eSim's Eeschema, the Verilog block is represented as a sub-circuit. Input sources are modeled using independent voltage sources with PULSE parameters to simulate a PDM stream.

V. Simulation and Results

A. Simulation Setup

The transient analysis parameters used in eSim are summarized in Table I.

TABLE I
SIMULATION PARAMETERS

Parameter	Value
Input Modulator Frequency	10.24 MHz
Decimation Ratio (N)	64
Output Data Rate	160 kHz
Internal Register Width	24-bit
Simulation Time	2 ms

B. Waveform Analysis

The results were extracted using the Python-based plotting tool integrated into eSim.

- **Input Waveform:** Represents a 1-bit PDM signal.

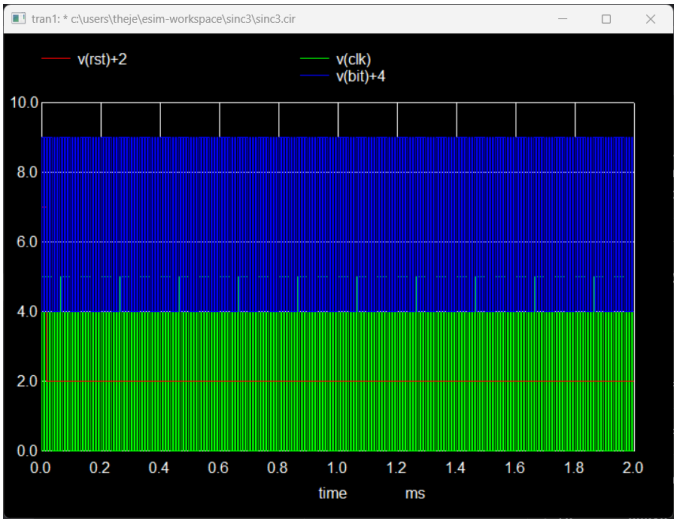

Fig. 1. Clk and bitstream

- **Output Waveform:** A 16-bit digital representation of the reconstructed signal.

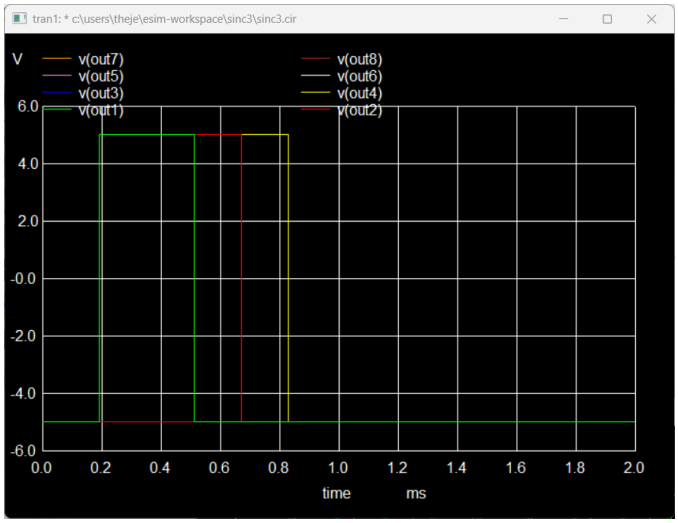

Fig. 2. Output Bits

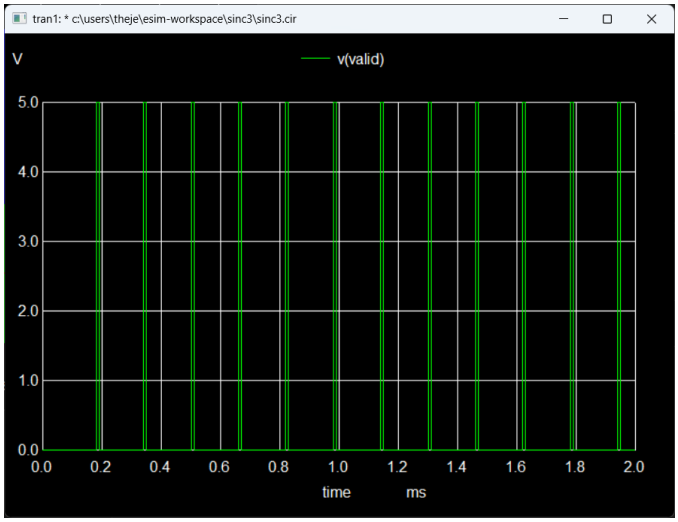

Fig. 3. Valid Bit

VI. Conclusion

The migration of the Sinc3 filter into eSim confirms the tool's robustness for digital VLSI research. The output waveforms verified against the classic model show that eSim provides an accurate environment for mixed-signal design. Future work could involve implementing the optimized two-stage low-power architectures as discussed in [4].

References

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