

Name of the participant : Lahari Tanneeru

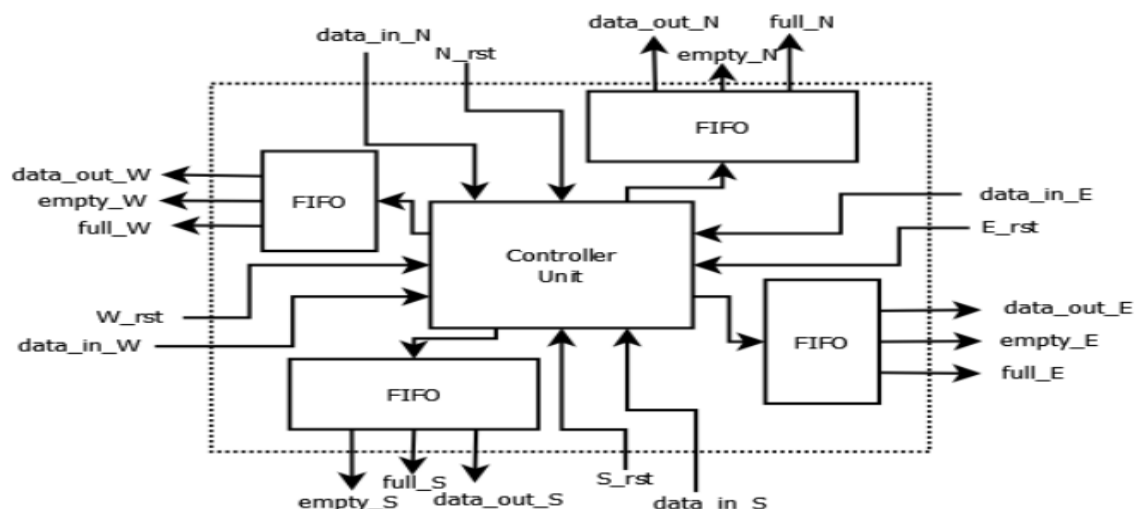
Affiliation / Institution : Rajiv Gandhi University of Knowledge technologies, Nuzvid

Title of the circuit : SIMULATION OF LOW AREA AND HIGH SPEED NINE PORT NETWORK-ON-CHIP ROUTER ARCHITECTURE

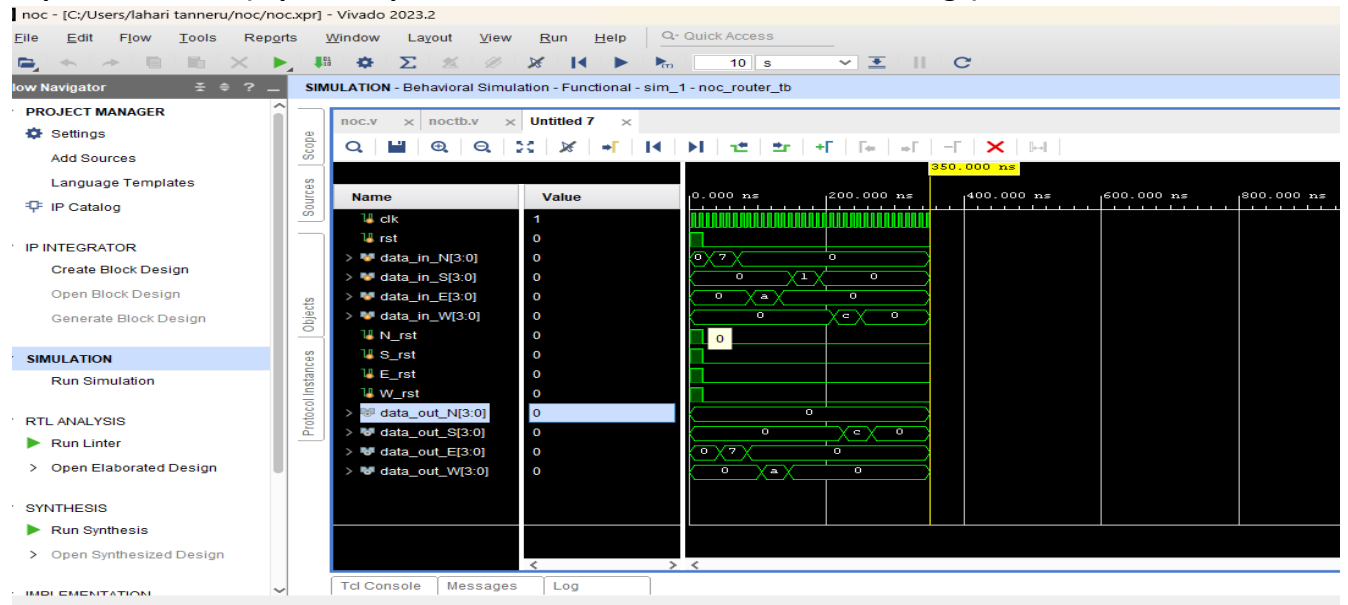
Theory/Description : The paper proposes a **low-area, high-speed nine-port Network-on-Chip (NoC) router** for efficient communication in multi-core systems. Traditional bus architectures fail to handle increasing data transfer between multiple processing elements, leading to reduced performance and scalability issues. To overcome this, the authors design a **3×3 mesh-based NoC router** that enables parallel data communication. The architecture consists of **routing logic, FIFO buffers, channel selection block, and controller unit**. It uses the **deterministic XY routing algorithm**, where data is first routed along the X-direction and then the Y-direction, ensuring shortest path transmission while avoiding deadlock and livelock. FIFO buffers temporarily store data and prevent congestion, while the controller manages data flow across four directions (North, South, East, West). Implemented using **VHDL and simulated in Xilinx tools**, the design achieves high speed (≈ 244 MHz) with reduced hardware resources, making it suitable for scalable and efficient NoC-based systems.

Expected Outcome/outputs : The designed 4-port NoC router successfully routes input packets to the required North, South, East, or West output ports based on direction bits. FIFO buffers prevent data loss, arbitration resolves conflicts, and registered outputs remove high-impedance states. The simulation confirms stable, correct packet transfer and reliable communication between interconnected router nodes.

Circuit Diagram(s) :

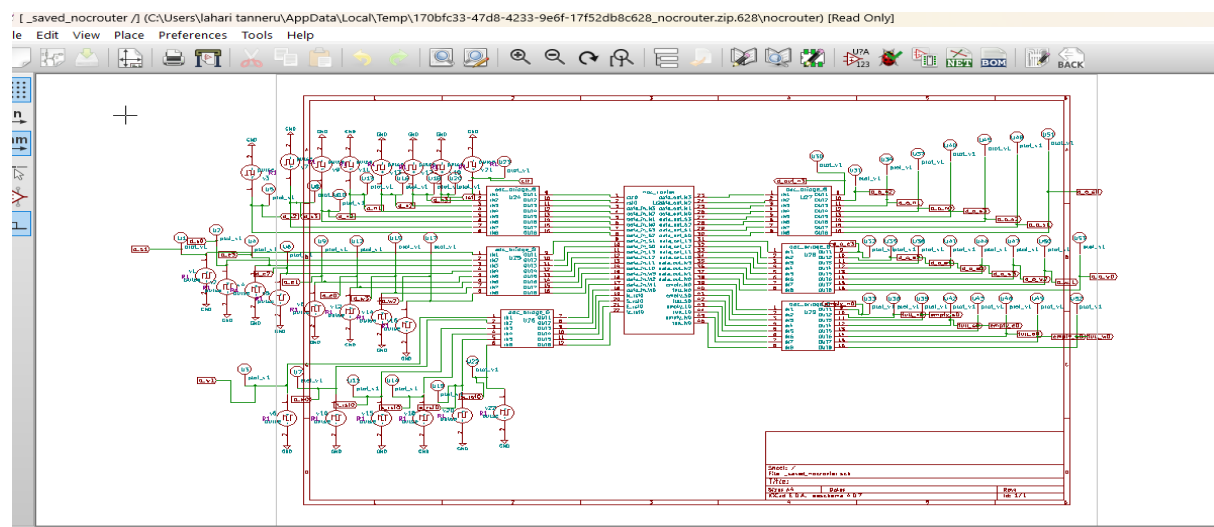


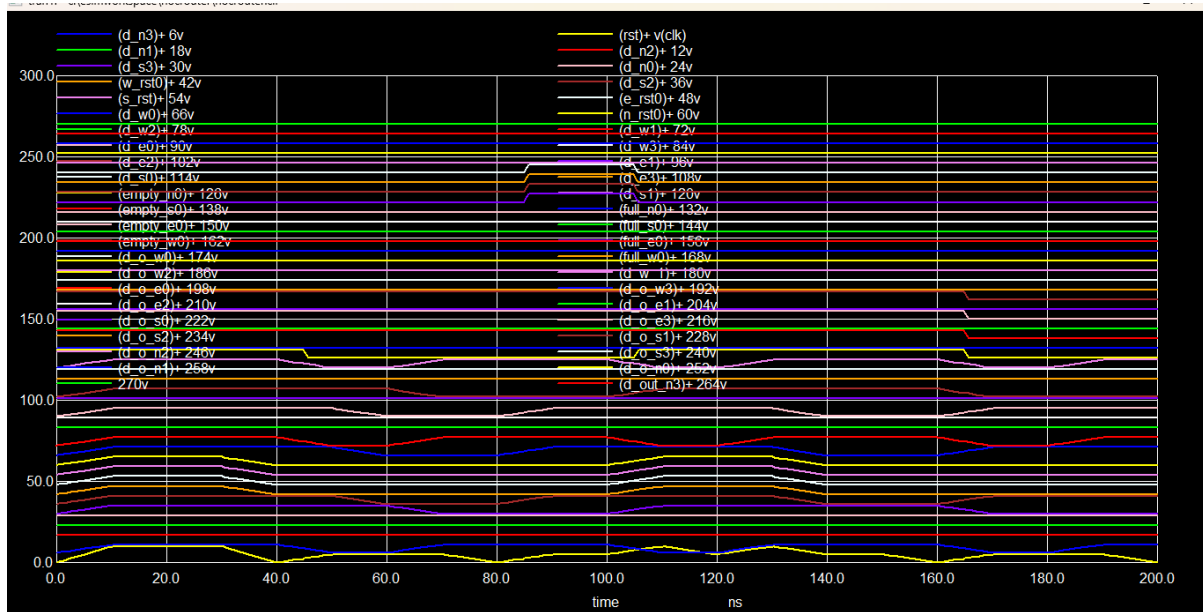
Expected Results (Input, Output waveforms and/or Multimeter readings) :



```
ngspice -p C:\eSimWorkspace\nocrouter\nocrouter.cir.out

Inside foo before eval.....
clk=1
rst=0
data_in_N=15
data_in_S=7
data_in_E=11
data_in_W=15
N_rst=0
S_rst=0
E_rst=0
W_rst=0
data_out_N=0
data_out_S=15
data_out_E=0
data_out_W=0
empty_N=0
full_N=0
empty_S=0
full_S=0
empty_E=0
full_E=0
empty_W=0
full_W=0
```





Research Paper/Journal/etc. : <https://doi.org/10.1109/RTEICT42901.2018.9012247>

Source/Reference(s) : • Route Packets, Not Wires: On-Chip Interconnection Networks, W. J. Dally and B. Towles.

- IEEE Xplore Digital Library, papers on NoC router design and arbitration.
- Xilinx Vivado User Guide for Verilog simulation and synthesis.