Simulation of a Soft-Switching Inspired Interleaved Boost Converter using SiC MOSFETs in eSim

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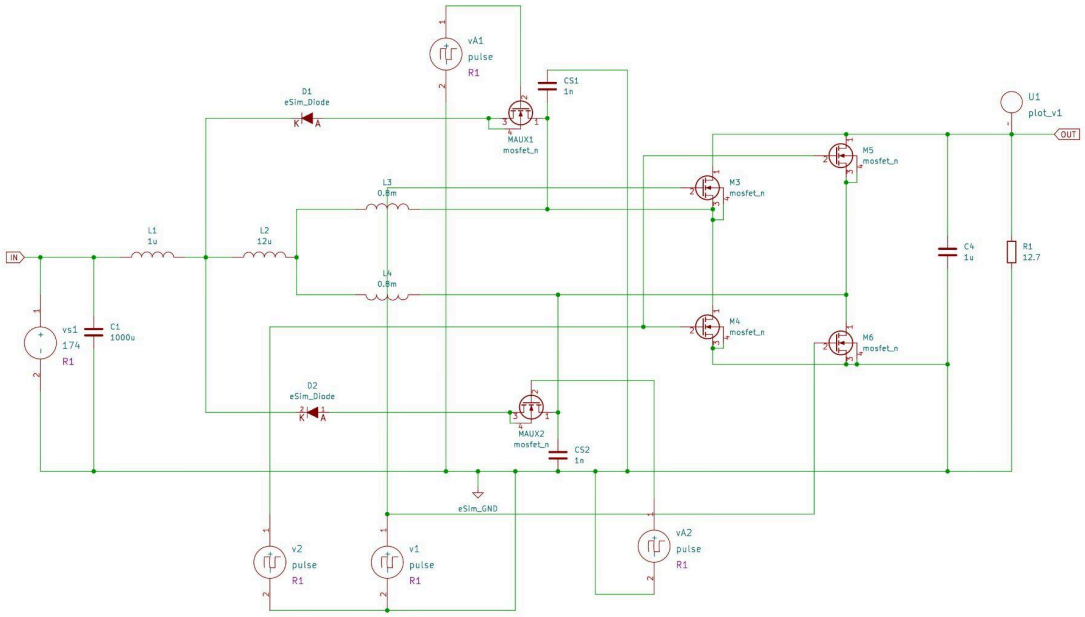
This work presents the simulation and analysis of a soft-switching Silicon Carbide (SiC) interleaved boost converter operating at 112 kHz. The converter uses a dual-phase interleaved topology combined with Snubber Assisted Zero Voltage and Zero Current Transition (SAZZ) to reduce switching losses and improve efficiency. The system boosts an input voltage of 174 V to 400 V at a power level of 12.5 kW. Two switching phases operate with a 180° phase shift, reducing ripple and improving dynamic performance. Soft-switching is achieved through an auxiliary circuit consisting of an auxiliary switch, diode, and resonant elements. The auxiliary switch turns on before the main switch, enabling:
Zero Voltage Switching (ZVS): Main switch turns on when voltage across it is zero.
Zero Current Switching (ZCS): Current through the switch is minimized at turn-on.
A resonant LC circuit formed by the auxiliary inductor and snubber capacitor enables controlled discharge of switch capacitance.
The voltage gain of the converter is given by:

$$V_{out} = \frac{V_{in}}{1 - D}$$

Interleaving doubles the ripple frequency and reduces input/output current ripple. The use of SiC devices allows high-frequency operation with improved efficiency and reduced losses.

Circuit Diagram



Symbols, and Values:

1. Source voltage- Vs1
2. Snubber capacitor: Cs1, Cs2: 1nF
3. Auxilary mosfets: Maux1, Maux2 (C2M0080120D)
4. Diode: D1, D2 (C4D40120D)
5. Phase 1 main switching leg mosfet: m3, m6 (CAS100H12AM1)
6. Phase 2 main switching leg mosfet: m4, m5 (CAS100H12AM1)
7. Input Capacitor: Cin1(1mF)
8. Output Capacitor: Cout1(1uF)

Component Values

All component values were selected based on high-frequency SiC operation and soft-switching requirements. The main boost inductance ensures sufficient energy storage, while the auxiliary inductance and snubber capacitance (1 nF) are tuned to enable resonant transition for ZVS. The input capacitor (1000 µF) stabilizes the DC source, and the output capacitor (1 µF) supports high-frequency ripple filtering.

Results / Output

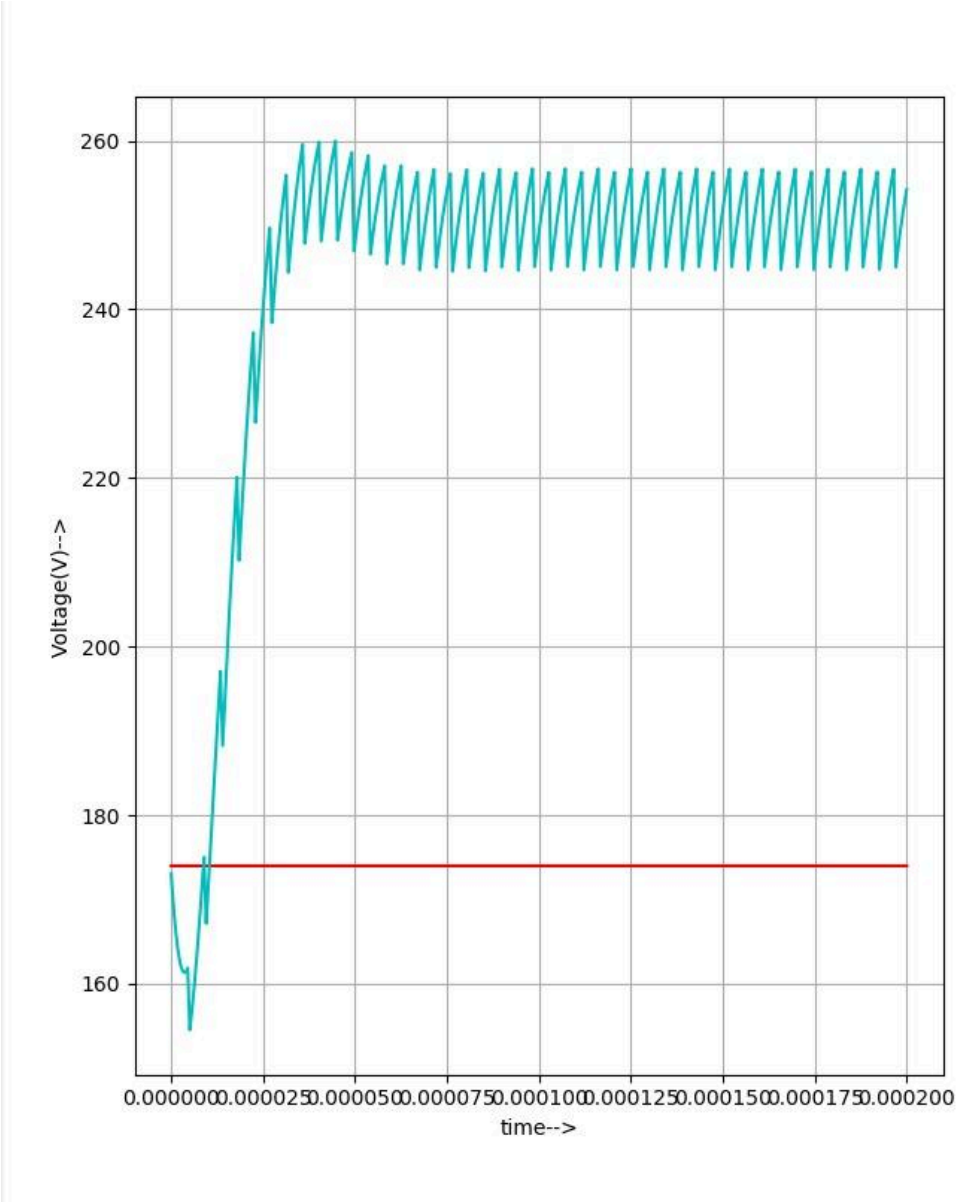


Fig: Vin and Vout Plot

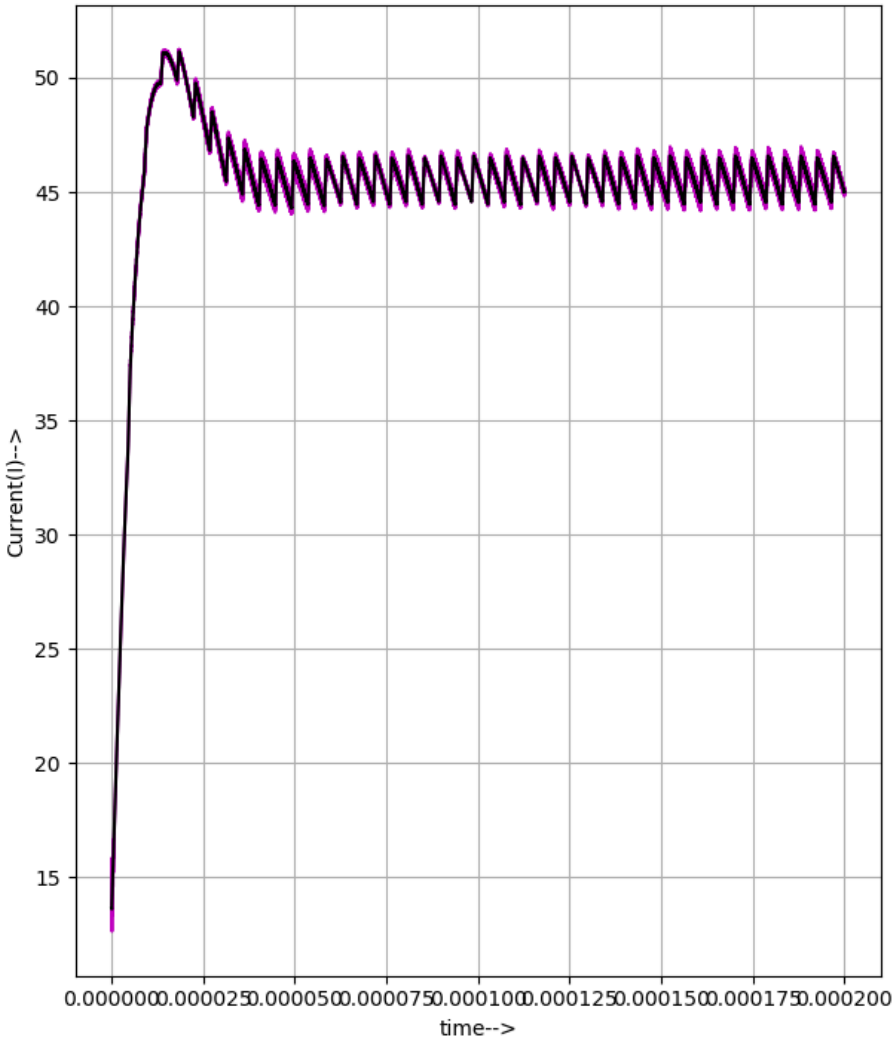


Fig: Inductor Current Waveforms - L1 and L2

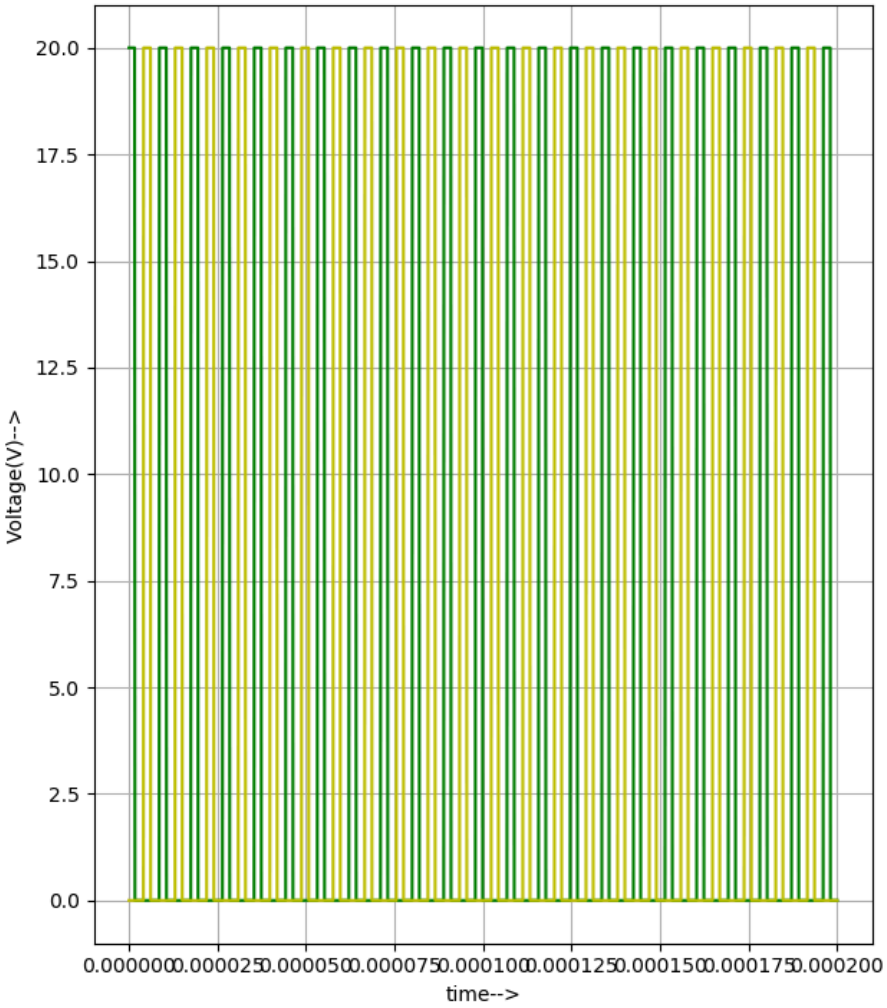


Fig: Switch voltages for Auxiliary MOSFETs

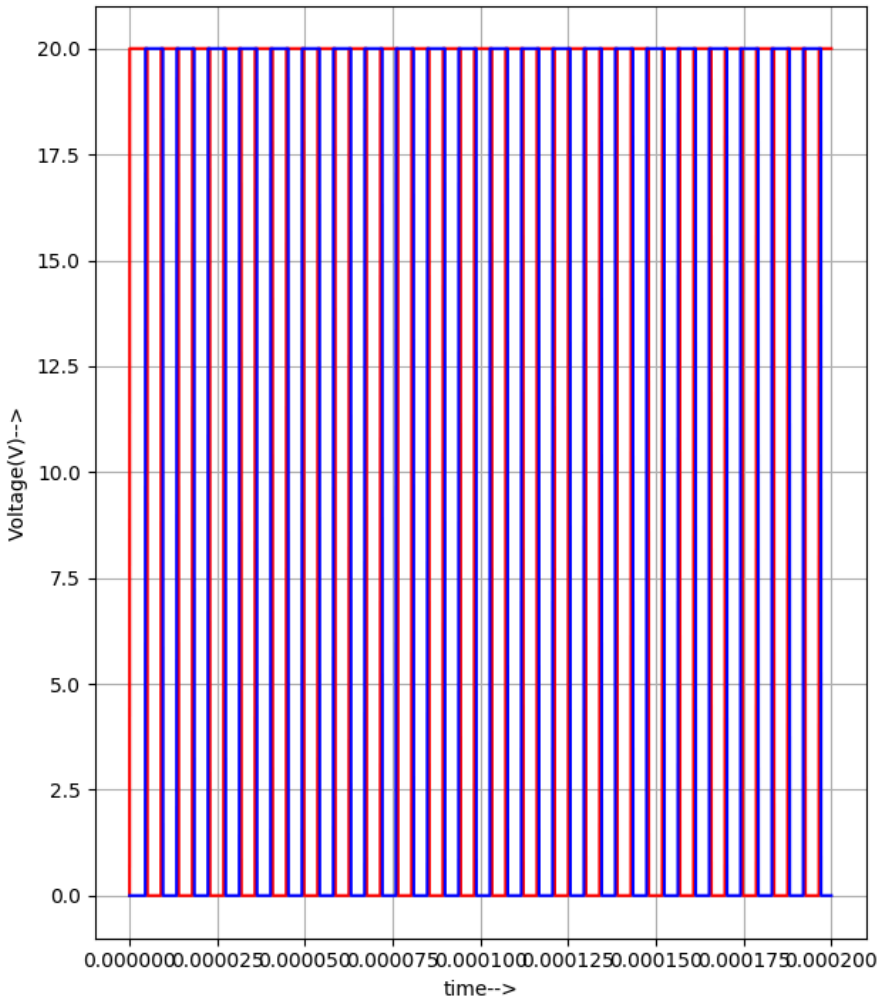


Fig: Main MOSFET legs switch voltages

Simulation was performed using ngspice under steady-state conditions.

Key observations:

- Output voltage achieved: ~260 V (lower than theoretical 400 V)
- Output current: ~20–21 A
- Ripple frequency: 224 kHz (due to interleaving)
- Estimated efficiency: ~95%

Soft-switching behavior (expected):

- Smooth voltage transition across switches
- Reduced dv/dt
- Resonant current in auxiliary branch

Reason for Deviation from Expected Output

The simulated output voltage (~260 V) is significantly lower than the theoretical value of 400 V, despite operating at the intended duty cycle of 56.5%. This discrepancy is attributed to incomplete energy transfer caused by improper interaction between the auxiliary soft-switching circuit and the main boost operation.

Although the snubber capacitance (1 nF) and auxiliary gate timing (0.4 μs advance) were set according to design specifications, waveform analysis indicates that the soft-switching mechanism is not functioning as intended. Instead of enabling efficient Zero Voltage Switching (ZVS), the auxiliary resonant path diverts a portion of the inductor current into local resonant oscillations.

As a result:

- The effective energy delivered to the output is reduced
- The average inductor current (~45 A) is significantly lower than the expected ~72 A
- The output voltage exhibits large ripple and fails to settle at the theoretical boosted level

This indicates that the converter is operating in a partially resonant regime rather than an ideal boost mode. Possible causes include improper resonance timing, parasitic interactions, or incomplete discharge of the snubber capacitor before main switch turn-on.

Therefore, the reduced output voltage is primarily due to inefficient power transfer caused by suboptimal soft-switching operation, rather than an error in duty cycle or component values.

Validation

The simulation results verify the fundamental operation of the interleaved boost converter:

1. The converter successfully operates in boost mode (Vout > Vin)
2. Interleaving of two phases results in increased ripple frequency (2× fsw) and reduced current stress per phase
3. The system demonstrates stable switching behavior at high frequency (112 kHz)

However, the output voltage stabilizes around 260 V instead of the expected 400 V, indicating non-ideal energy transfer. Analysis shows that:

1. The average inductor current is lower than the theoretical requirement
2. The auxiliary soft-switching network introduces parasitic resonant energy circulation
3. This reduces the net power delivered to the load

Thus, while the topology and switching scheme are functionally correct, the soft-switching mechanism is not fully optimized, leading to deviation from ideal boost performance.

References

1. IEEE Paper - https://ieeexplore.ieee.org/document/7104462
2. eSim User Manual
3. NGSpice Documentation