Abstract

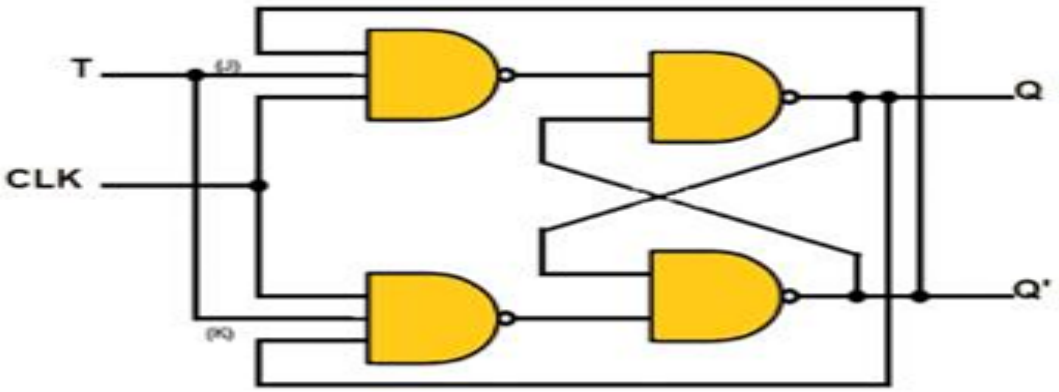
Title: Design and Implementation of T Flip-Flop using JK Flip-Flop

Theory/Description:
A T (Toggle) Flip-Flop is a fundamental sequential circuit used in digital electronics that changes its state (toggles) on every clock pulse when the input T is high. It can be efficiently implemented using a JK Flip-Flop by connecting both J and K inputs together, making them act as a single toggle input. This configuration eliminates the invalid state present in SR Flip-Flops and ensures stable operation.

Explanation:

1. In this implementation, the J and K inputs of the JK Flip-Flop are shorted together and treated as a single input T. This allows the flip-flop to toggle its output when T = 1.
2. When T = 0, both J and K inputs become 0, and the flip-flop holds its previous state without any change.
3. When T = 1, both J and K inputs become 1, causing the flip-flop to toggle its output state (i.e., from 0 to 1 or from 1 to 0) at each clock edge.
4. The circuit operates synchronously with the clock signal, meaning the output changes only at the triggering edge of the clock pulse.
5. This design is widely used in counters and frequency division applications due to its predictable toggling behavior.

Sample Circuit Diagram:

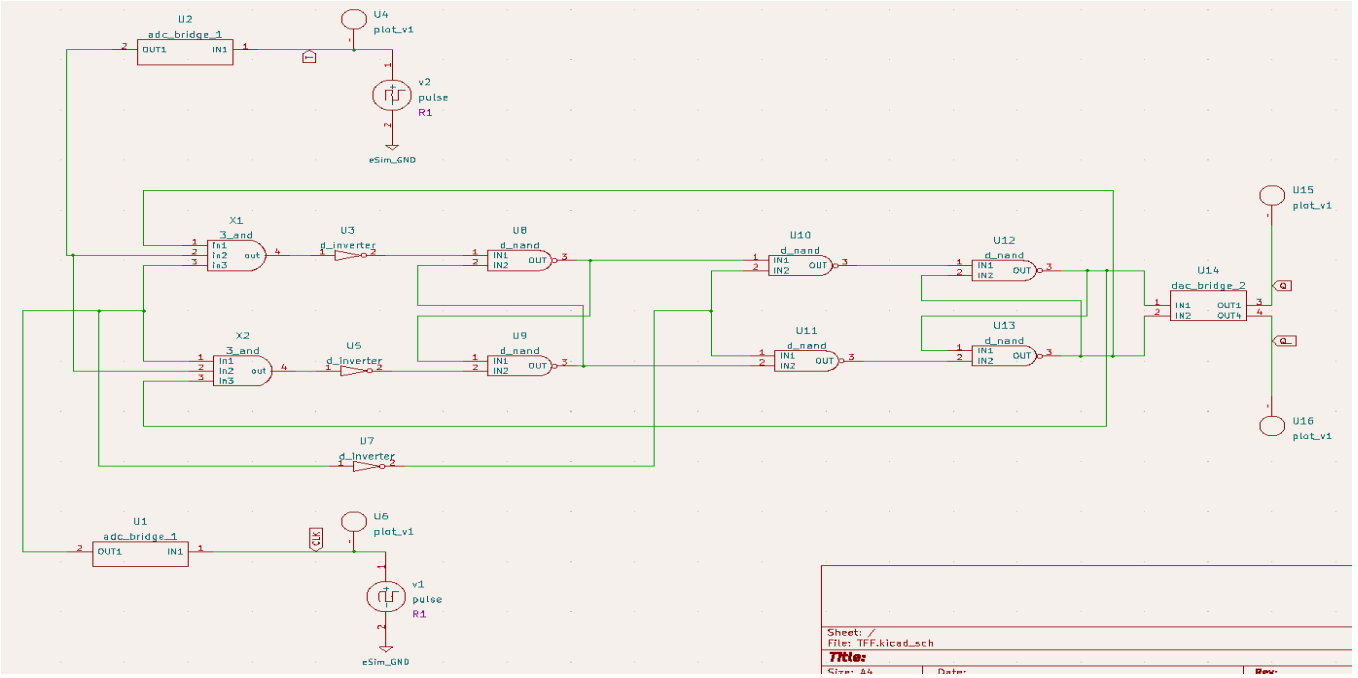


Applications:

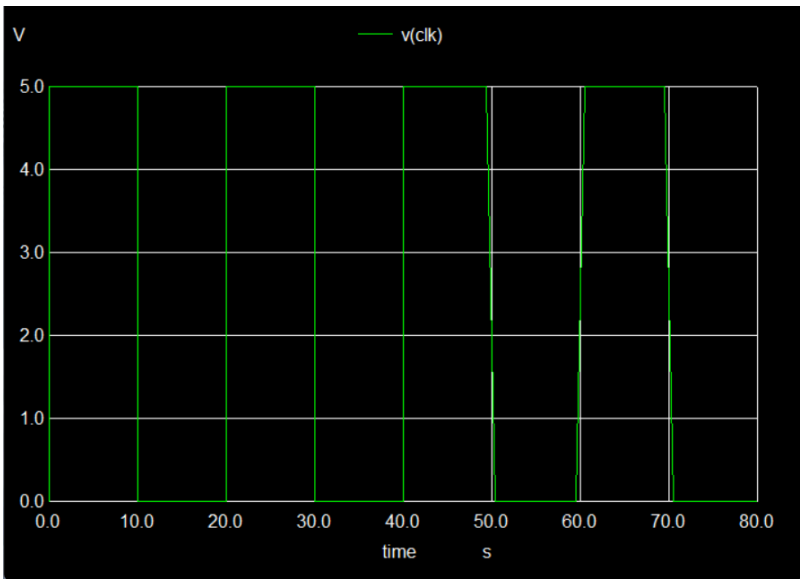
1. T Flip-Flops are widely used in digital counters (such as ripple counters and synchronous counters) where the toggling behavior helps in counting sequences efficiently.

2. They are used as frequency dividers, where the output frequency becomes half of the input clock frequency, making them useful in clock generation circuits.
3. T Flip-Flops act as basic memory elements in sequential circuits, storing one bit of information and maintaining state until the next clock pulse.
4. They are used in timing circuits and control units where periodic state changes are required based on clock signals.
5. T Flip-Flops are also used in shift registers and digital systems for designing finite state machines and control logic.

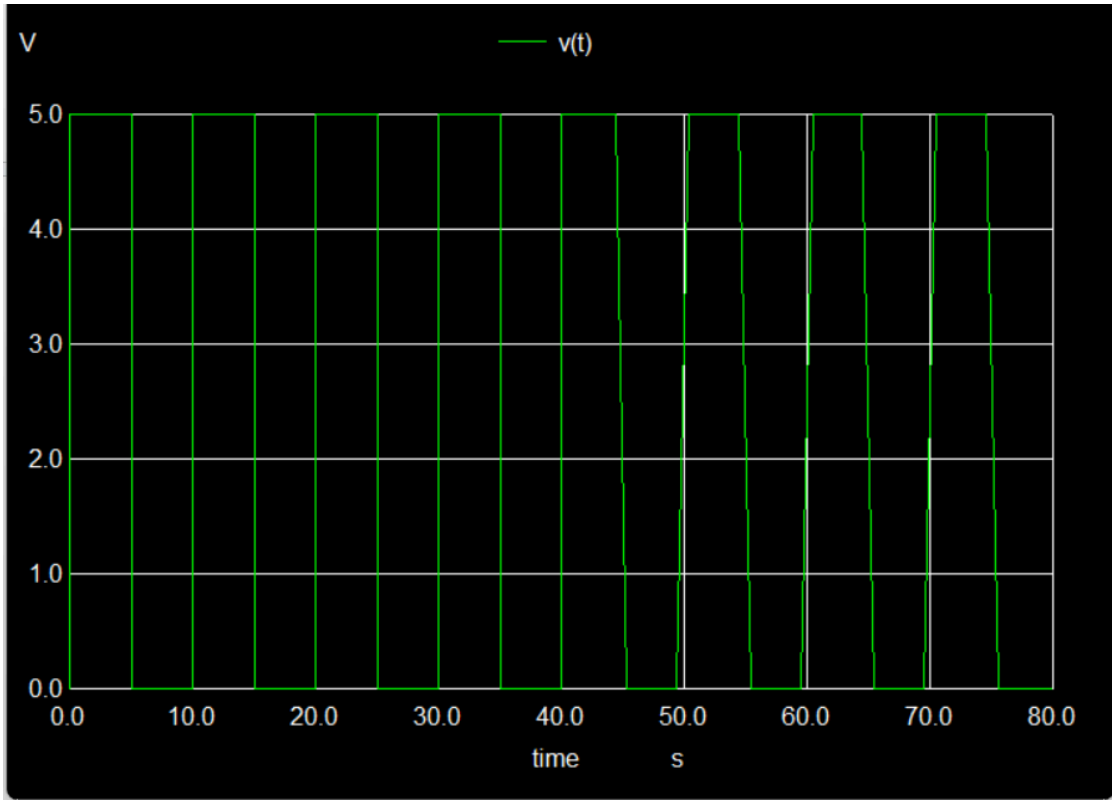
Circuit Diagram:



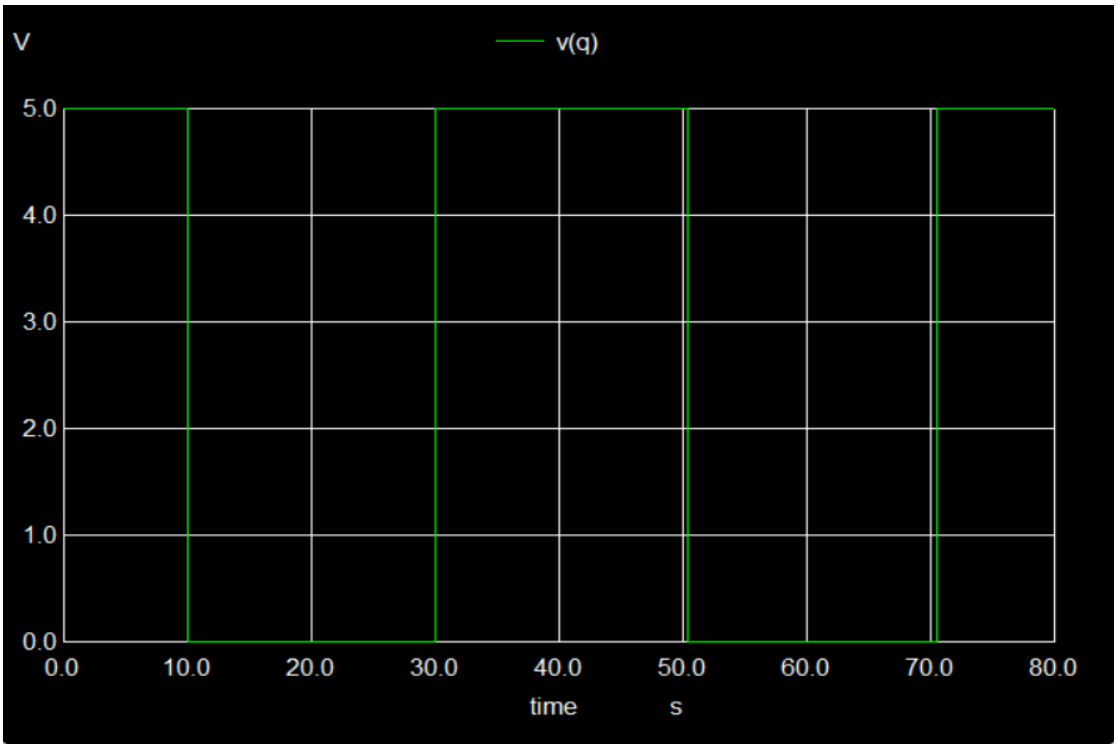
Results/Output: Ngspice Plots:
Clock:



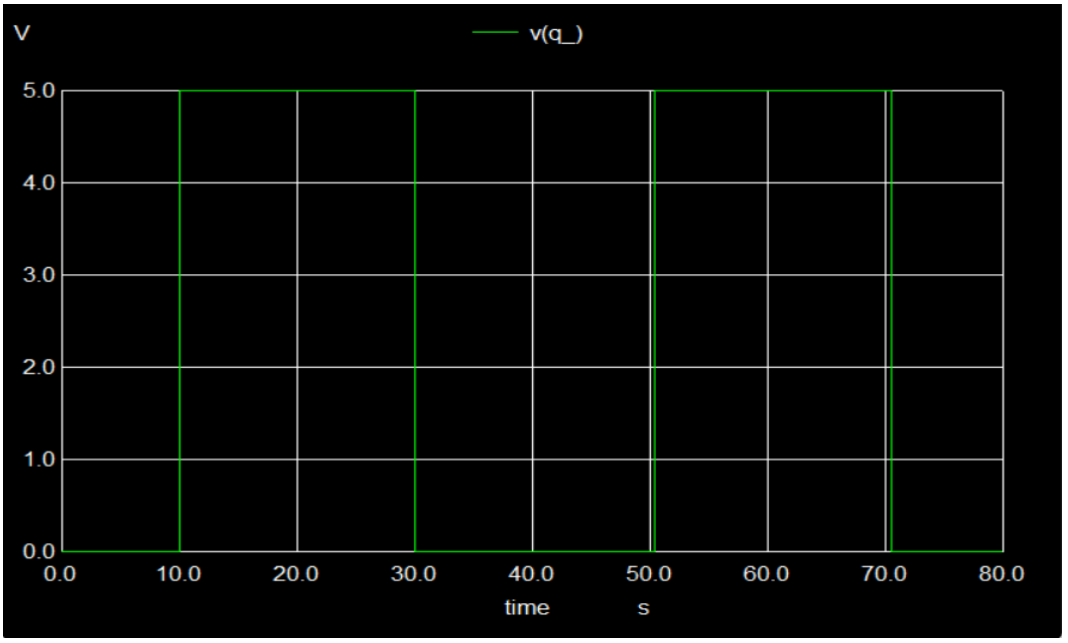
T:


V
v(t)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

Q:

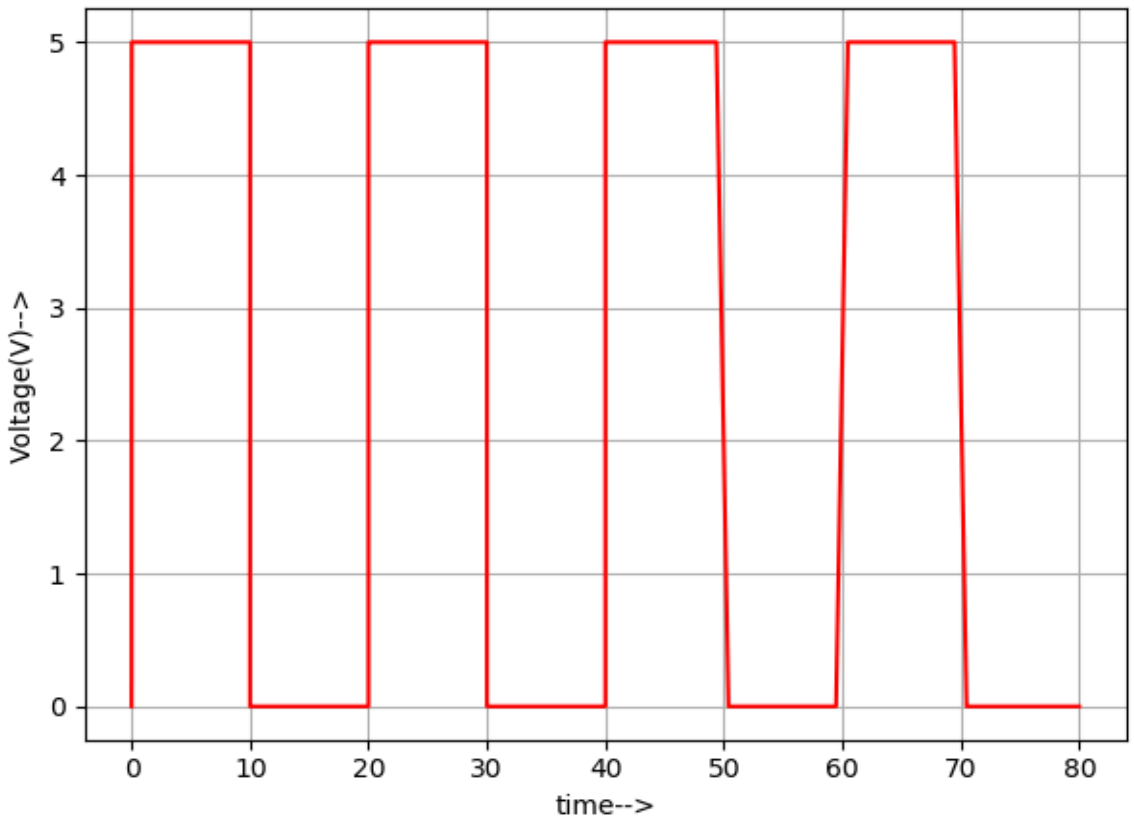

V
v(q)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

Q_ :

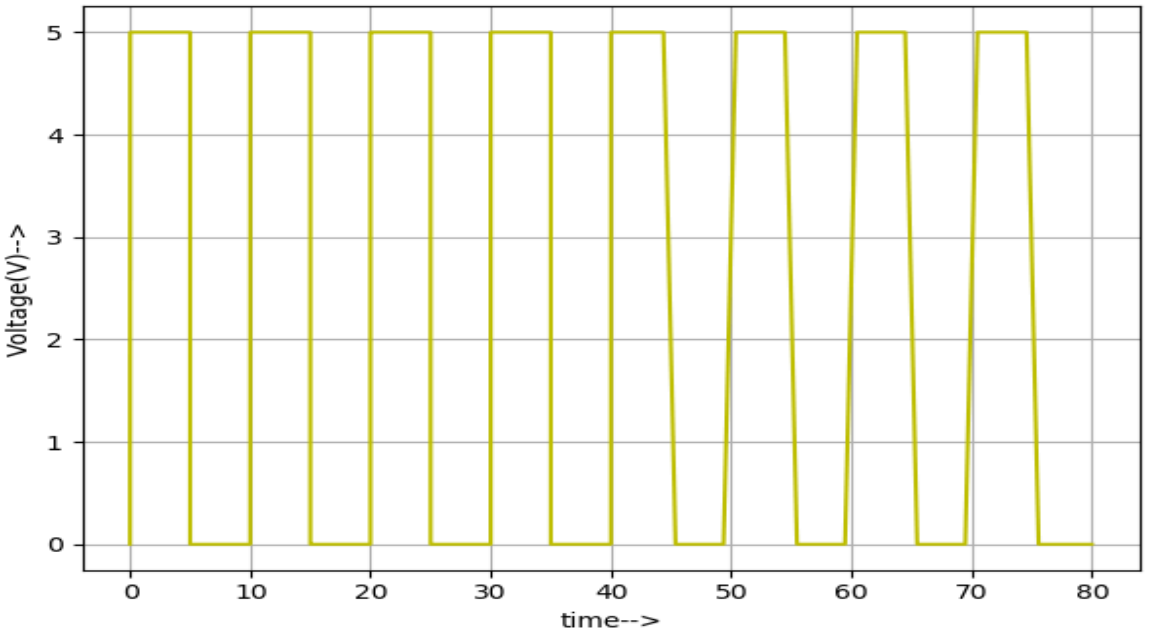


Python Plots:

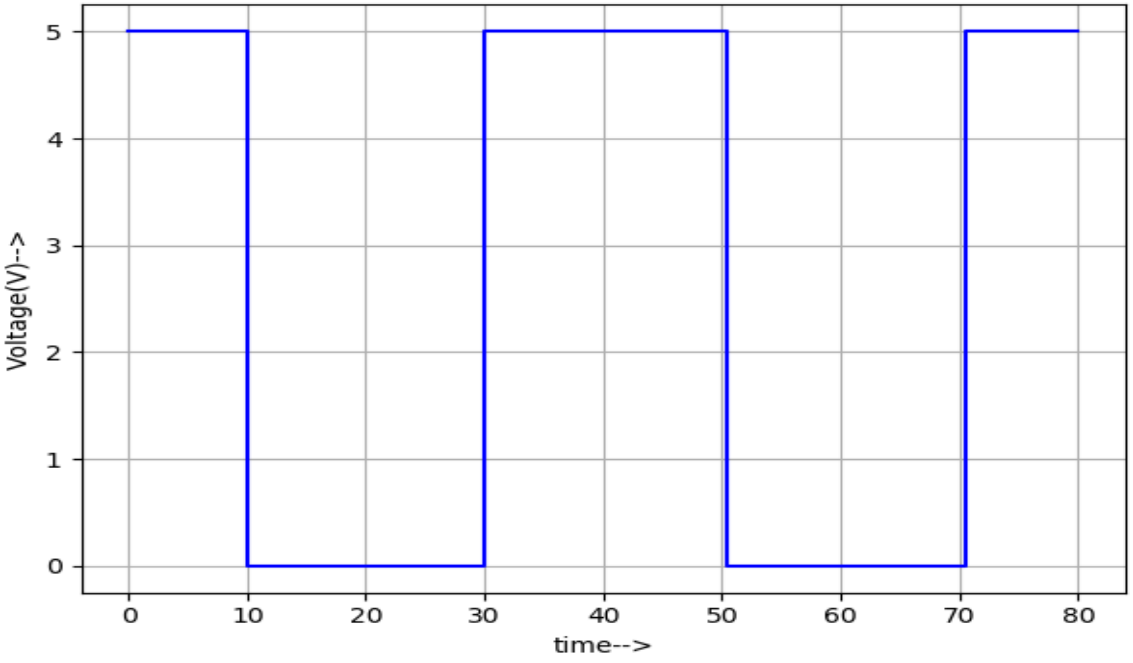
Clock:



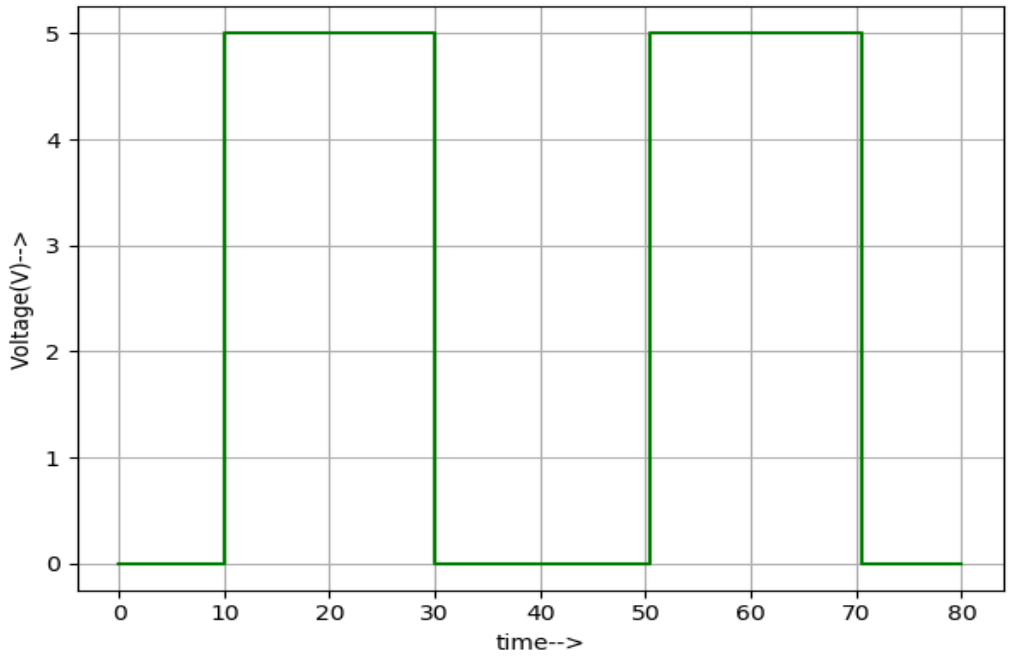
T:


Voltage(V)-->
time-->
0
1
2
3
4
5
0
10
20
30
40
50
60
70
80

Q:


Voltage(V)-->
time-->
0
1
2
3
4
5
0
10
20
30
40
50
60
70
80

Q_:



References:

1.Title : Designing an Efficient Approach for JK and T Flip-Flop with Power Dissipation Analysis Using QCA

Author : Shraddha Pandey, Sonali Singh and Subodh Wairya
Link:https://www.researchgate.net/publication/304991620_Designing_an_Efficient_App roach_for_JK_and_T_Flip-Flop_with_Power_Dissipation_Analysis_Using_QCA

2.Title : A Study of JK and T Flip-Flops with and without Delay Using QCA

Author : Aditi Bal, Subhashree Basu, Supriyo Sengupta

Link: https://www.iosrjournals.org/iosr-jvlsi/papers/vol4-issue6/Version 1/K04617076.pdf