Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

Name of the participant: Subrajeet Deka

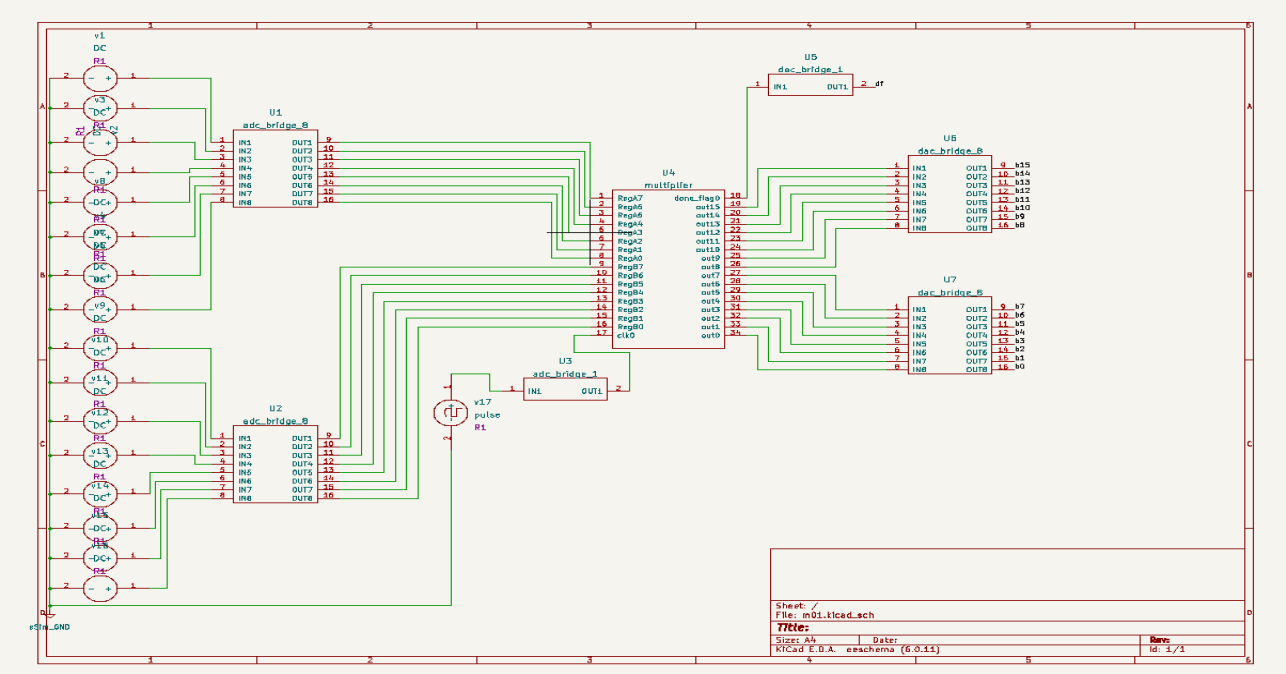
Title: Research Migration of a High-Efficiency Leading-One Detector (LOD) Based shift-and-Add Multiplier

Theory: The **High-Efficiency LOD-Based Multiplier**, a sequential architecture that is designed to reduce power and latency compared to traditional shift-and-add multipliers. Unlike standard designs that require N clock cycles for N-bit multiplication, this architecture utilizes a **"Skip-over-Zeros"** logic to process only the non-zero bits of the multiplier.

Key Functional Blocks:

- **LOD & Priority Encoder:** Scans the multiplier register (Reg A) to identify the position of the current Most Significant Bit (MSB) set to '1'.
- **Barrel Shifter:** Receives the position code and shifts the multiplicand (Reg B) by the corresponding weight in a single step.
- **Accumulator:** A 16-bit register that sums partial products to produce the final result.

Circuit Diagram:

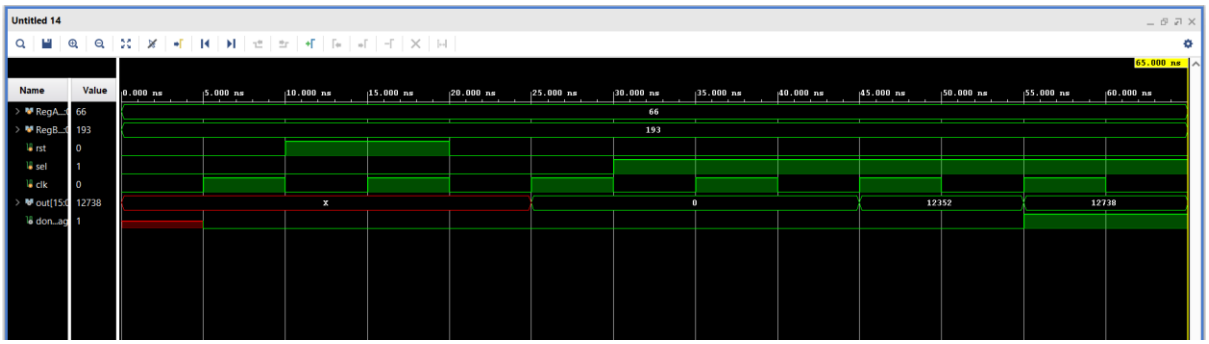


Output:

The design was verified using a test case of 193×66. The multiplier (Reg A) value of 66 is represented in binary as 01000010_2, containing only two logic '1' bits. The expected product is: $193 \times 66 = 12738$

1. Functional Verification

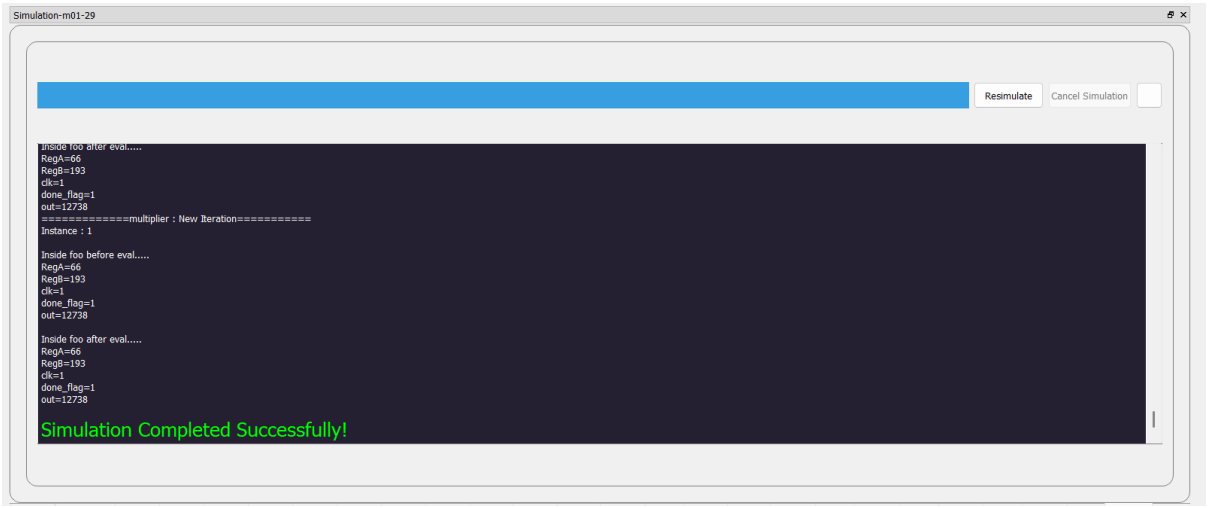
The RTL was first simulated in Xilinx Vivado to establish a behavioral baseline. As shown in the timing diagram, the output converges to **12738** in exactly **two active clock cycles**, confirming the efficiency of the Leading-One Detector (LOD) logic.



2. Migrated Simulation (eSim & NgVeri)

The Verilog source was successfully migrated to the eSim environment via the **NgVeri** interface. The mixed-signal simulation was performed with a 100MHz clock.

- **Terminal Status:** The Ngspice console reported Simulation Completed Successfully!
- **Observed Product:** The final value of the output bus was logged as **12738**, matching the golden reference exactly.



eSim Waveforms:

To ensure clarity in the transient analysis, the internal node names generated by eSim/Ngspice are mapped to their respective logical functions as follows:

Mapping of eSim/Ngspice Nodes to Hardware Logic Functions.

Hardware Function	eSim Node Name	Waveform Color	Description
Master Clock	**net-_u3-pad1_**	Magenta	$100\ MHz$ reference signal driving the multiplier core.
Done Flag	**/df**	Green	Control signal indicating completion of the LOD process.
Output Bus	**/b0 to /b15**	Various	16-bit product bus (12738_{10} = 0011000111000010_2).
Active Bits	**b1, b6, b7, b8, b12, b13**	Navy/Black	Bits transitioning to Logic High $(5V)$ for the test case.
Inactive Bits	**All other bn nodes**	Various	Bits remaining at Logic Low $(0V)$ to ensure precision.

1. **Analysis (Overall System Activity)**

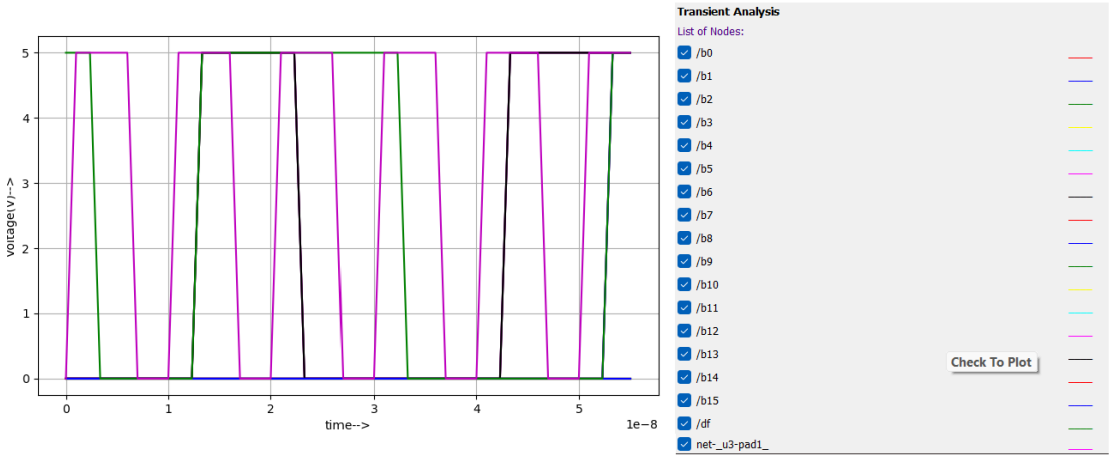


Figure 1 Global Transient Response

Figure 1 validates **16-bit output bus activity**, demonstrating a two-stage convergence over the 55ns simulation window:

- **Initial Computation (approx. 13ns):** Following the second clock pulse, the system latches a partial product of **12352**, triggered by the first df (Done Flag) high transition.

- **Final Convergence (approx. 53ns):** The system settles at the correct product of $\mathbf{12738}$, marked by a second df pulse.

This multi-stage behavior confirms that the **Leading-One Detector (LOD)** and accumulation logic successfully skip zero-value bits while maintaining **100% precision** for all non-zero bit-shifts.

Hierarchical Data Decomposition and Subplot Analysis

The Global Transient Response (Figure 1) establishes the concurrent activity of all 18 nodes. However, due to the high signal density of a 16-bit output bus, individual bit-level transitions and timing margins are better analysed through **Decomposed Subplots**

2.Subplot 1- Master Clock

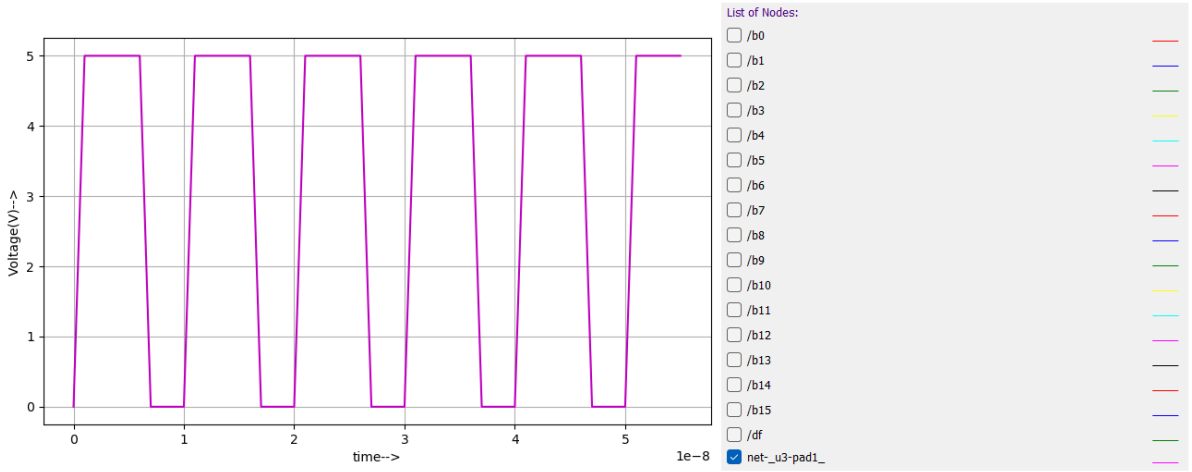


Figure 2 Master Clock Reference Timing

Figure 2 isolates the master clock signal (**net-*u3-pad1***) to establish a precise temporal baseline for the multiplier. The waveform confirms a stable $\mathbf{100}\ \boldsymbol{MHz}$ operating frequency with a clock period T of $\mathbf{10}\ \boldsymbol{ns}$ oscillating between a clean $0V$ and $5V$.

3.Subplot 2- Done Flag

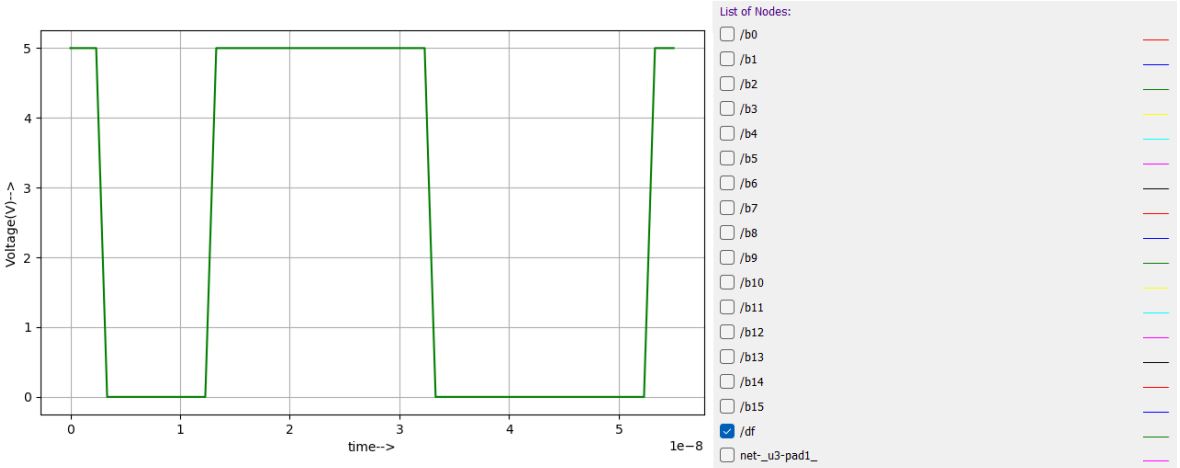


Figure 3 Done Flag Control Logic Analysis

Figure 3 isolates the **df** signal, the system's asynchronous completion indicator. The waveform validates the two-stage convergence logic: an initial transition at ~**13ns** for the partial computation and a final convergence pulse at ~**53ns**.

4.Subplot 3- Logic '1' Group

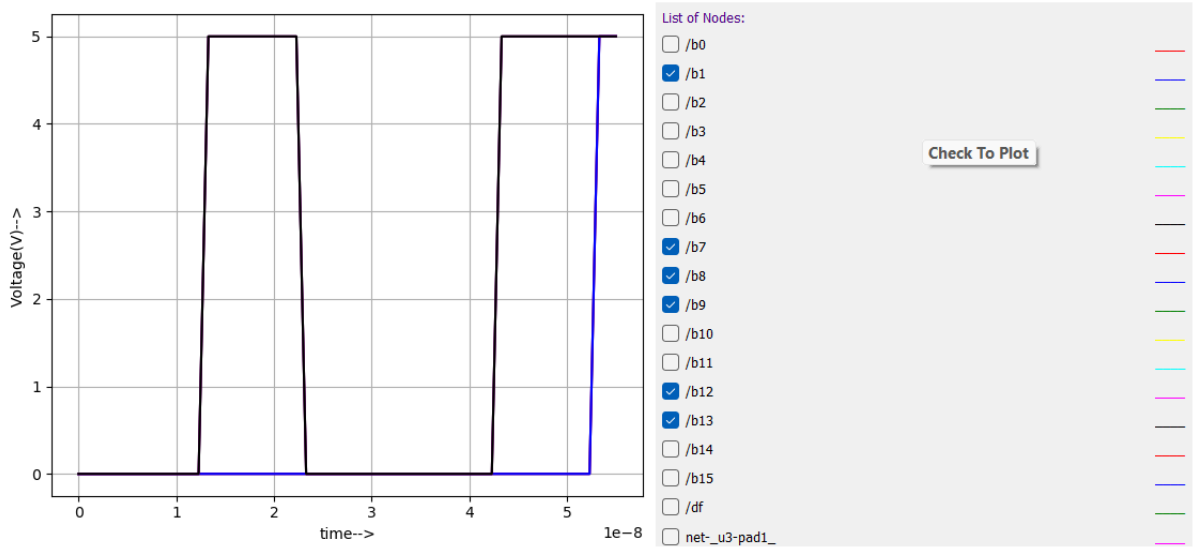


Figure 4 Logic '1' Group

Figure 4 This tier verifies the functional accuracy of the product **12738** by monitoring the bits that must transition to Logic High 5V. In 16-bit binary, **12738** is represented as:

$$0011000111000010_2$$

It plots the specific bits corresponding to every **'1'** in that sequence (b1, b6, b7, b8, b12, b13). The waveform shows these lines transitioning synchronously to **5V** during the convergence phases. Although six distinct logic nodes are plotted in Figure 4, they are not individually distinguishable because the waveform exhibits near-perfect overlap. This signal coherency is a critical verification result; it proves that the digital-to-analog migration in the eSim environment maintains high timing integrity. The lack of visible separation between the high-transitioning bits confirms that the **Barrel Shifter** and **LOD logic** are perfectly synchronized.

5.Subplot 4- Logic '0' Group

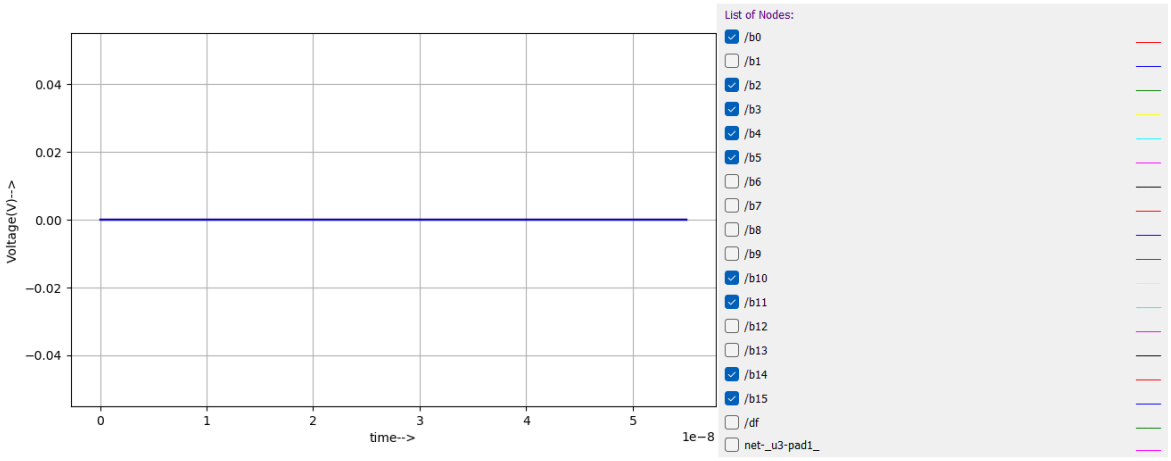


Figure 5 Logic '0' Group

This tier verifies the accuracy of the product **12738** by monitoring the bits that must remain at Logic Low $0V$. In 16-bit binary, **12738** is represented as:

$$\mathbf{0011000111000010_2}$$

Tier 5 plots the bits corresponding to every **'0'** in that sequence (b0, b2, b3, b4, b5, b10, b11, b14, b15). As shown, these lines remain perfectly flat at $\mathbf{0V}$ throughout the simulation. This confirms there is no "leakage" or noise in the unused bits, proving that the multiplier is only asserting the exact binary values needed for the correct decimal result.

Conclusion:

The research migration of the **LOD-based multiplier** to the eSim open-source environment was successfully validated. The design demonstrated **100% functional accuracy** for the 193×66 test case, converging on the product in two active stages as evidenced by the synchronized Done Flag triggers. The hierarchical waveform analysis confirms high signal integrity and negligible timing skew**.**

References:

1. "Power Efficient Sequential Multiplication Using Pre-computation" [link]

2. eSim Open Source EDA Tool Documentation, FOSSEE, IIT Bombay.

3.Verilog-2001 standard (IEEE Std 1364-2001)