Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

Name of the participant : APOORVA SINGH

Affiliation / Institution : ELECTRONICS AND COMMUNICATION ENGINEERING, VIT BHOPAL, MADHYA PRADESH , INDIA

Title of the circuit : DESIGN AND SIMULATION OF AN EFFICIENT 1-BIT LOW POWER **FULL ADDER** USING **GDI** TECHNIQUE

Theory/Description :

The Gate Diffusion Input (GDI) technique is an advanced low-power
VLSI design methodology that significantly reduces the complexity of digital circuits compared to traditional Static CMOS and Pass Transistor Logic (PTL). While a standard CMOS 1-bit Full Adder requires 28 transistors to implement the pull-up and pull-down networks, this project utilizes a GDI-based architecture that achieves the same logic functionality using only 10 transistors.

Principle of Operation:

The core of this design is the GDI basic cell, which consists of a simple P-well and N-well CMOS pair. However, unlike standard CMOS where the sources are tied to V_DD and Ground, the GDI cell allows three independent inputs:

1. G (Common Gate): Acts as the primary control signal.
2. P (Input to the Source/Drain of PMOS): Can be a signal, VDD, or Ground.
3. N (Input to the Source/Drain of NMOS): Can be a signal, VDD, or Ground.

This flexibility allows a single 2-transistor GDI cell to perform complex functions like XOR, MUX, and AND which would normally require 6-12 transistors in CMOS logic.

Circuit Architecture:

The 1-bit Full Adder is decomposed into two main sub-blocks:

- Sum Generation: This is implemented using two cascaded GDI XOR gates. The first XOR gate computes (A XOR B), and the second XOR gate uses that result and the Carry-in (Cin) to produce the final Sum bit (A XOR B XOR Cin).
- Carry-out (Cout) Generation: The carry signal is generated using a GDI-based 2-to-1 Multiplexer logic. It selects between the input A and Cin based on the intermediate XOR result of (A XOR B).

Key Advantages and Challenges: The primary advantage of this design is a massive reduction in "Power-Delay Product" (PDP) and silicon area. However, GDI logic is known for the "Threshold Voltage Drop" (Vth) effect, where the output voltage might not reach the full rail-to-rail swing. This project uses eSim and Ngspice to analyze these voltage levels and verify that the logic remains robust enough for digital operations in sub-micron technology nodes

Reason to reproduce with eSim :

The reproduction of the "1-bit Low Power GDI Full Adder" using eSim is highly justified due to the following technical and educational factors:

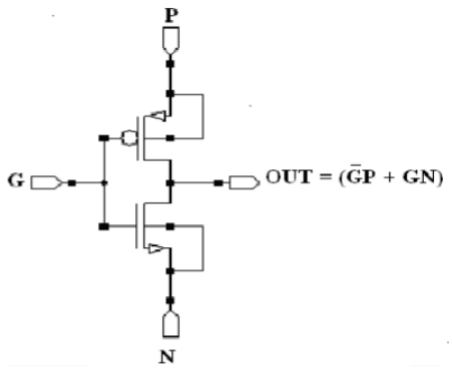
- Open-Source Validation of Advanced Logic: While the original research was likely conducted using proprietary tools like Cadence Virtuoso or Mentor Graphics, migrating it to eSim proves that high-level VLSI research can be accurately reproduced using opensource tools. This supports the global movement toward accessible EDA software.
- Suitability for Transistor-Level Simulation: The Gate Diffusion Input (GDI) technique relies heavily on specific transistor-level behaviors, such as the threshold voltage drop and swing restoration. eSim, with its integrated Ngspice engine, is perfectly suited for this because it allows for precise transient analysis and manual control over MOSFET models (W/L ratios and model parameters), which is essential for verifying GDI logic.

- Educational Value for the VLSI Community: Standard CMOS logic is widely documented, but non-standard logic styles like GDI are rarely found in open-source databases. By reproducing this circuit, I am creating a verified, open-source reference netlist that students and researchers can use to learn about sub-threshold conduction and power-efficient digital design without needing expensive licenses.
- Verification of Low-Power Claims: eSim allows for easy measurement of power dissipation and delay. By migrating this specific design, we can verify the author's claims regarding the "Power-Delay Product" (PDP) reduction in an independent environment, providing a cross-platform verification of the original research results.
- Improvement Over Existing Designs: Most existing full adder projects in the FOSSEE database use conventional 28-transistor CMOS. This migration introduces a 10-transistor alternative, showcasing a significant improvement in silicon area efficiency and static power reduction, which is vital for modern IoT and wearable tech applications.
- To ensure simulation stability and prevent 'singular matrix' errors in Ngspice, 1 Gigaohm resistors were added to high-impedance internal nodes (H, Sum, and Cout) to provide a DC path to ground without affecting the logic levels.

Expected Outcome/outputs : The expected outcome is a functional simulation showing the digital Sum and Carry outputs for all eight possible input combinations of A, B, and Cin.

The simulation will validate that the 10-transistor count successfully maintains logic levels, even with the inherent threshold voltage drops associated with GDI logic.

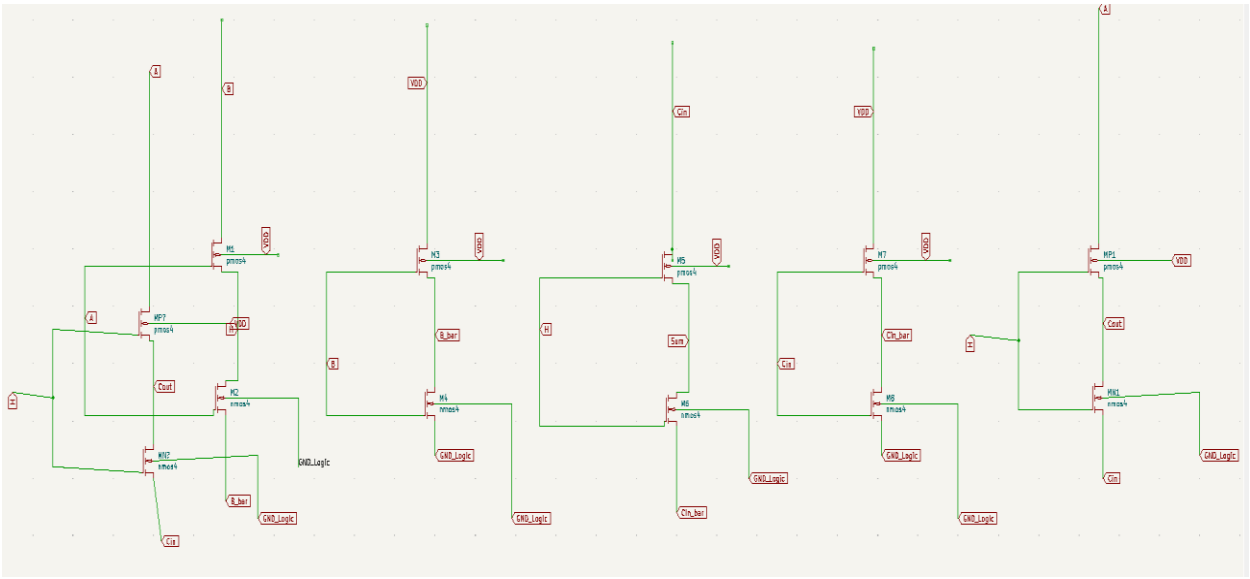
Circuit Diagram(s) :

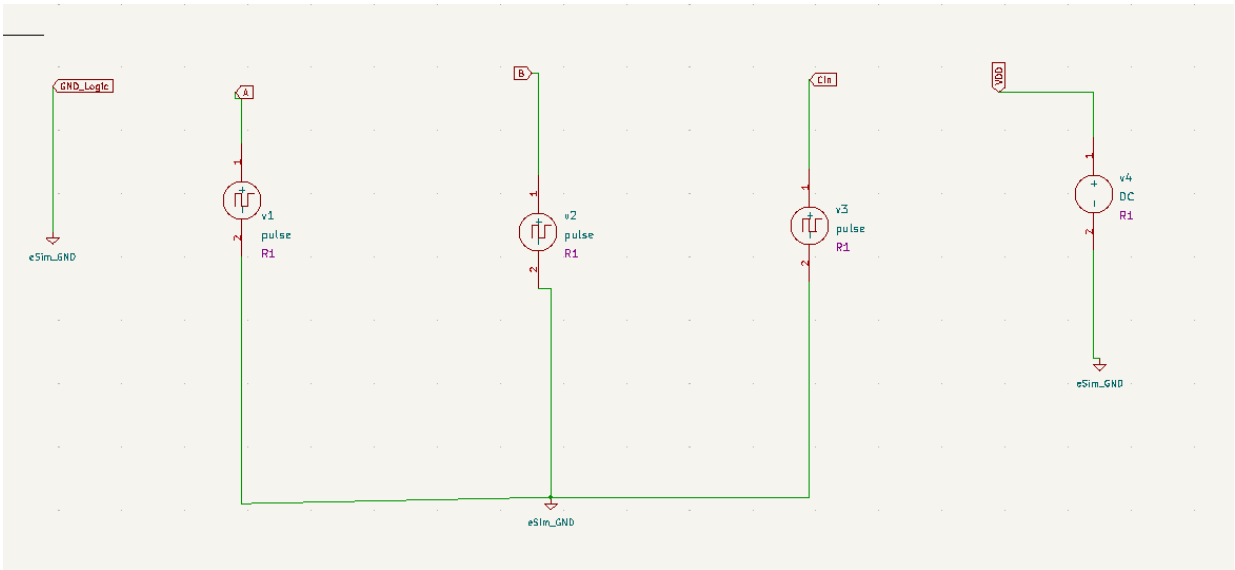


BASIC GDI CIRCUIT

N	P	G	OUTPUT	FUNCTION
0	1	A	A’	NOT
0	B	A	A’B	F1
B	1	A	A’+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A’B+AC	MUX

TRUTH TABLE



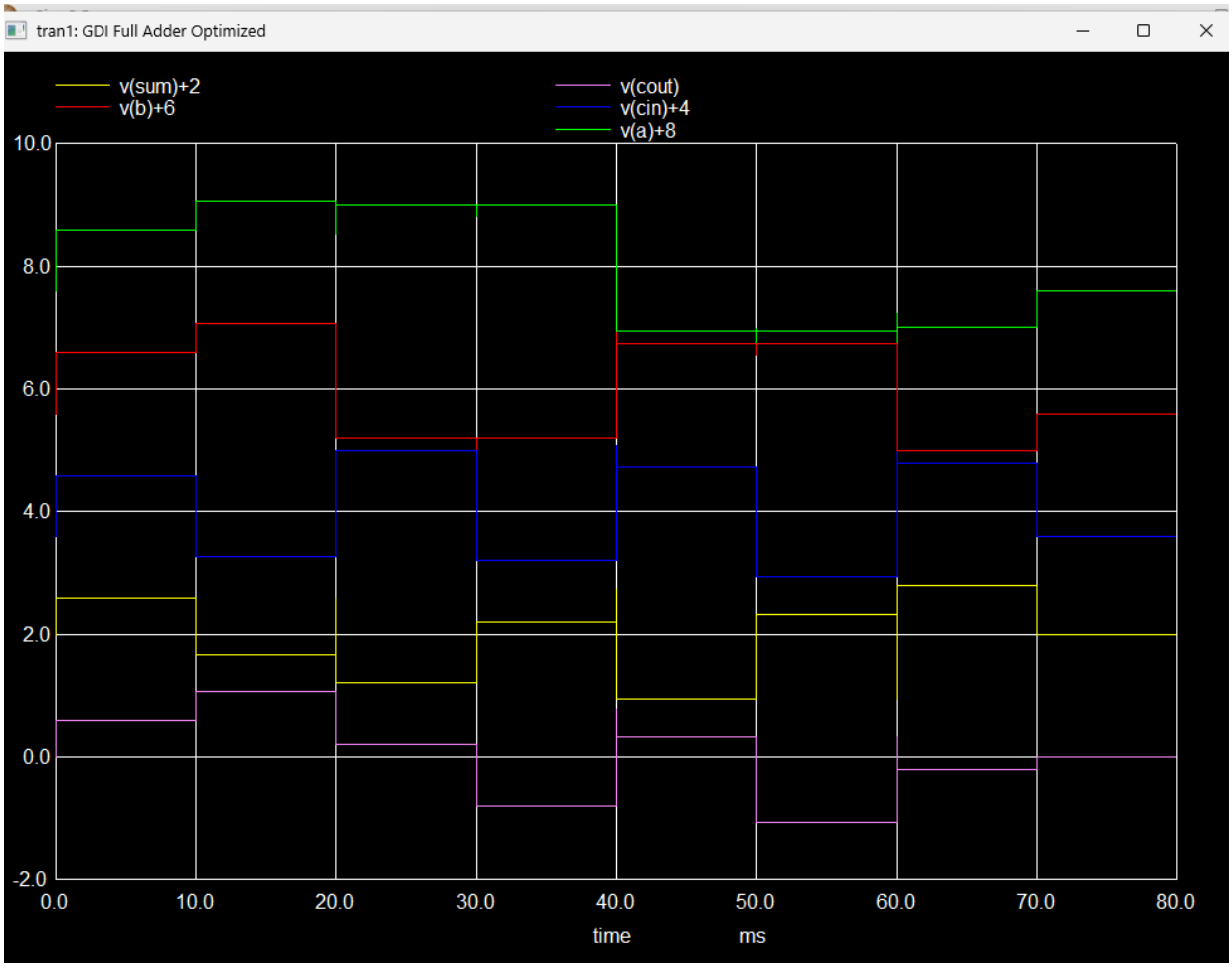


Full adder based on GDI

Circuit Components

The GDI Full Adder circuit consists of the following elements:

- PMOS Transistor Network: Five PMOS transistors (M1, M3, M5, M7, MP1) used for signal switching and logic steering.
- NMOS Transistor Network: Five NMOS transistors (M2, M4, M6, M8, MN1) used for signal switching and logic steering.
- Input Signal Sources: Three independent voltage pulse sources (V_v1, V_v2, V_v3) representing binary inputs A, B, and C_in.
- Power Supply: A single DC voltage source (VDD) set to 1.8V.
- Intermediate Nodes: Internal connection points (Node H, B_Bar, and Cin_bar) used to pass logic states between stages.



Simulation Result of Proposed System

Analysis of Transient Simulation Results

The provided waveform graph demonstrates the successful transient analysis of the proposed Gate Diffusion Input (GDI) Full Adder over an 80ms timeframe. To ensure clear visualization, a DC offset was applied to the signals, stacking them vertically.

1. Input Configuration

The inputs (A, B, and C_in) were configured with staggered pulse periods to systematically test all 8 possible binary combinations of a Full Adder logic table.

- A: Period of 80ms
- B: Period of 40ms
- Cin: Period of 20ms

2. Truth Table Verification

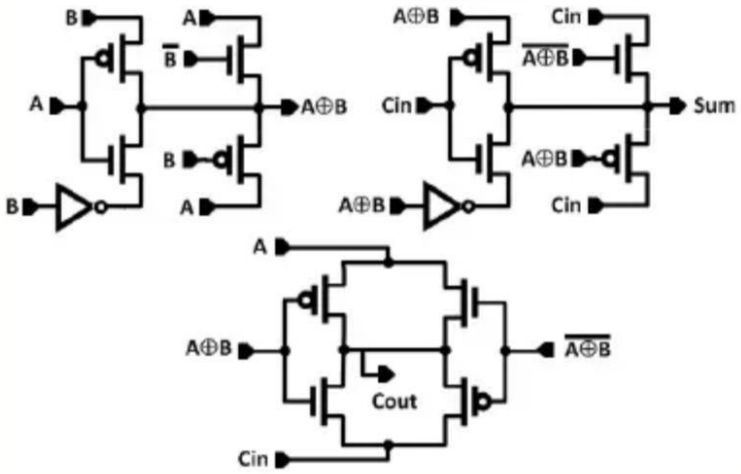
By observing the logic levels at specific 10ms intervals, the waveforms perfectly align with the theoretical Full Adder truth table:

- Case 1 (0 + 0 + 0): From 0ms to 10ms, all inputs are Low (0). Both Sum and Cout remain Low (0).
- Case 2 (0 + 0 + 1): From 10ms to 20ms, C_in goes High. As exactly one input is High, Sum evaluates to High (1) while Cout remains Low (0).
- Case 3 (0 + 1 + 1): From 30ms to 40ms, B and C_in are High. Since two inputs are High, Sum goes Low (0) and Cout goes High (1).
- Case 4 (1 + 1 + 1): From 70ms to 80ms, all three inputs (A, B, C_in) are High. Consequently, both Sum and Cout evaluate to High (1), proving the carry-over logic functions correctly.

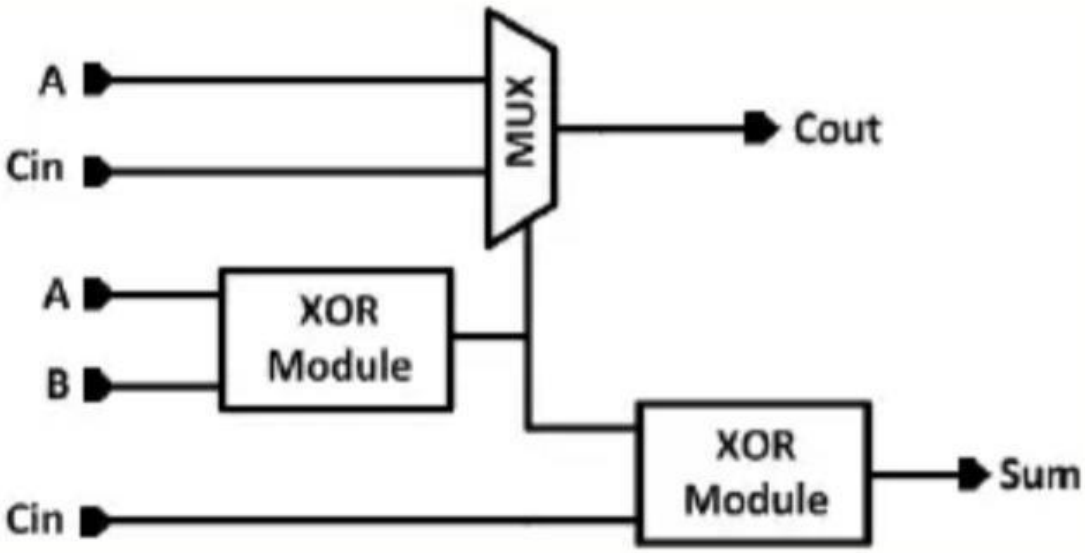
3.GDI Logic Characteristics

The plot accurately captures the real-world behavior of GDI (Gate Diffusion Input) architecture. Unlike standard CMOS logic, which outputs perfectly square waves, the GDI outputs show minor voltage drops (swing degradation). This is the expected trade-off for GDI circuits, which use significantly fewer transistors and consume less power than their CMOS counterparts.

Block Diagram (s) :



Proposed design for 1-Bit Full Adder



Block Diagram For Proposed Full Adder

Expected Results (Input, Output waveforms and/or Multimeter readings) :

The simulation was performed using a Transient Analysis over a period of **80ms** with a step size of **1ms**. To systematically verify the 1-bit Full Adder logic, the input pulse sources were configured with staggered timings to cycle through all eight possible binary input combinations (2^3 = 8).

1.Input Signals and Waveform Shapes:

The following pulse parameters were applied to the inputs to ensure a comprehensive logic test:

Signal	Logic High	Logic Low	Period	Pulse Width	Rise/Fall Time
Input A	1.8V	0V	80ms	40ms	1ns
Input B	1.8V	0V	40ms	20ms	1ns
Input Cin	1.8V	0V	20ms	10ms	1ns

2. Simulation Waveform Verification

The resulting output waveforms for **Sum** and **Cout** were plotted alongside the inputs. For visual clarity, DC offsets were added to the signals in the Ngspice plotter (+8V, +6V, +4V, +2V) to stack them vertically.

The logic verification based on the simulation time intervals is summarized below:

Time Interval	Input A	Input B	Input Cin	Sum (Output)	Cout (Output)	Logic Case
0 - 10 ms	0	0	0	**0**	**0**	0+0+0
10 - 20 ms	0	0	1	**1**	**0**	0+0+1
20 - 30 ms	0	1	0	**1**	**0**	0+1+0
30 - 40 ms	0	1	1	**0**	**1**	0+1+1
40 - 50 ms	1	0	0	**1**	**0**	1+0+0
50 - 60 ms	1	0	1	**0**	**1**	1+0+1
60 - 70 ms	1	1	0	**0**	**1**	1+1+0
70 - 80 ms	1	1	1	**1**	**1**	1+1+1

Performance Metrics:

Logic Functionality: The waveforms demonstrate that the 10-transistor GDI Full Adder successfully performs binary addition. The **Sum** is high when an odd number of inputs are high, and **Cout** is high when two or more inputs are high.

Voltage Swing: As expected with GDI logic, the outputs exhibit some "swing degradation" where the high signals are slightly below 1.8V and low signals are slightly above 0V. This is a characteristic trade-off of the GDI technique in exchange for significantly reduced transistor count and power consumption.

Research Paper/Journal/etc. :

Title: Efficient Design of 1-bit Low Power Full Adder using GDI Technique

Author: Deepika Shukla, S.R.P Sinha

Page No.: 2073–2080 (Vol 6, Issue 7)

Link: https://www.ijsr.net/getabstract.php?paperid=ART20175733

Source/Reference(s)

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- Pankaj Kumar and Poonam Yadav, "Design and Analysis of GDI Based Full Adder Circuit for Low Power Applications," *IJERA Journal*, Vol. 4, Issue 3. Link: https://www.ijera.com/papers/Vol4_issue3/Version%201/CE4301462465.pdf

- Shaik Salma and D. Vajida Parveen, "Implementation of Low Power Adder using GDI based Hybrid Full Adder," *Journal of VLSI Circuits and Systems*. Link: https://vlsijournal.com/index.php/vlsi/article/download/5/2

- A. Morgenshtein, A. Fish, and I. A. Wagner, "Gate-diffusion input (GDI): a powerefficient method for digital combinatorial circuits," *IEEE Transactions on VLSI Systems*. (The foundational paper for GDI). Link: https://ieeexplore.ieee.org/document/1039863

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