Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

Name of the participant : Chockalingam M

Affiliation / Institution : Department of Instrumentation Engineering / Madras Institute of Technology, anna University.

Title of the circuit : **High Speed CMOS-Based Comparative Design of Low Drop-Out Voltage Regulator.**

Theory/Description : A Low Drop-Out (LDO) Voltage Regulator is a linear regulator designed to operate with a very small difference between input and output voltage. The proposed research paper implements an LDO using CMOS technology with a folded cascade error amplifier and current buffer compensation technique to improve gain, stability, and power efficiency.

Reason to reproduce with eSim : The original LDO design is implemented using Cadence, a proprietary tool that is not easily accessible for all users. Reproducing the circuit in eSim provides an open-source and cost-effective platform for simulation, making it suitable for academic and research purposes. It enables a clear understanding of CMOS analog circuit behavior, including voltage regulation, stability, and transient response .

Expected Outcome/outputs : The expected outcome of the simulation is a stable and regulated output voltage of approximately for the given input conditions. The circuit should exhibit a smooth transient response during startup and load variations, with minimal overshoot or undershoot. Proper compensation ensures that the system operates without oscillations, thereby maintaining stability. Overall, the simulation demonstrates the fundamental behavior of a CMOS-based LDO regulator, including feedback control and voltage regulation.

Circuit Diagram(s) :

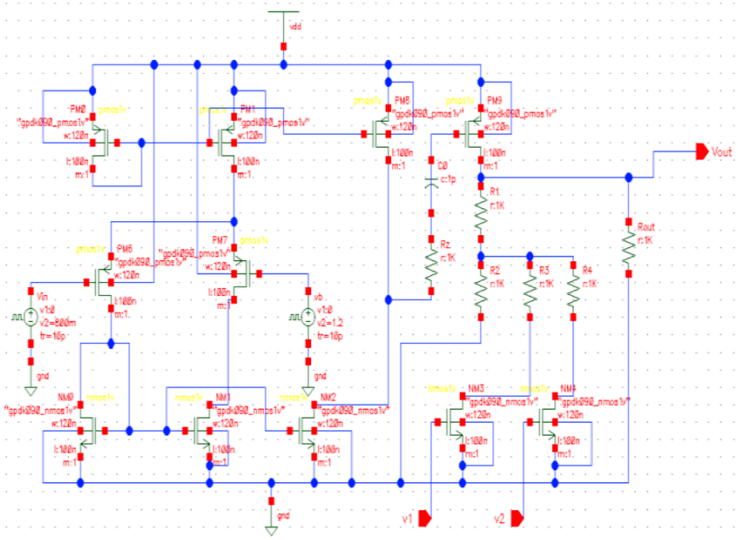
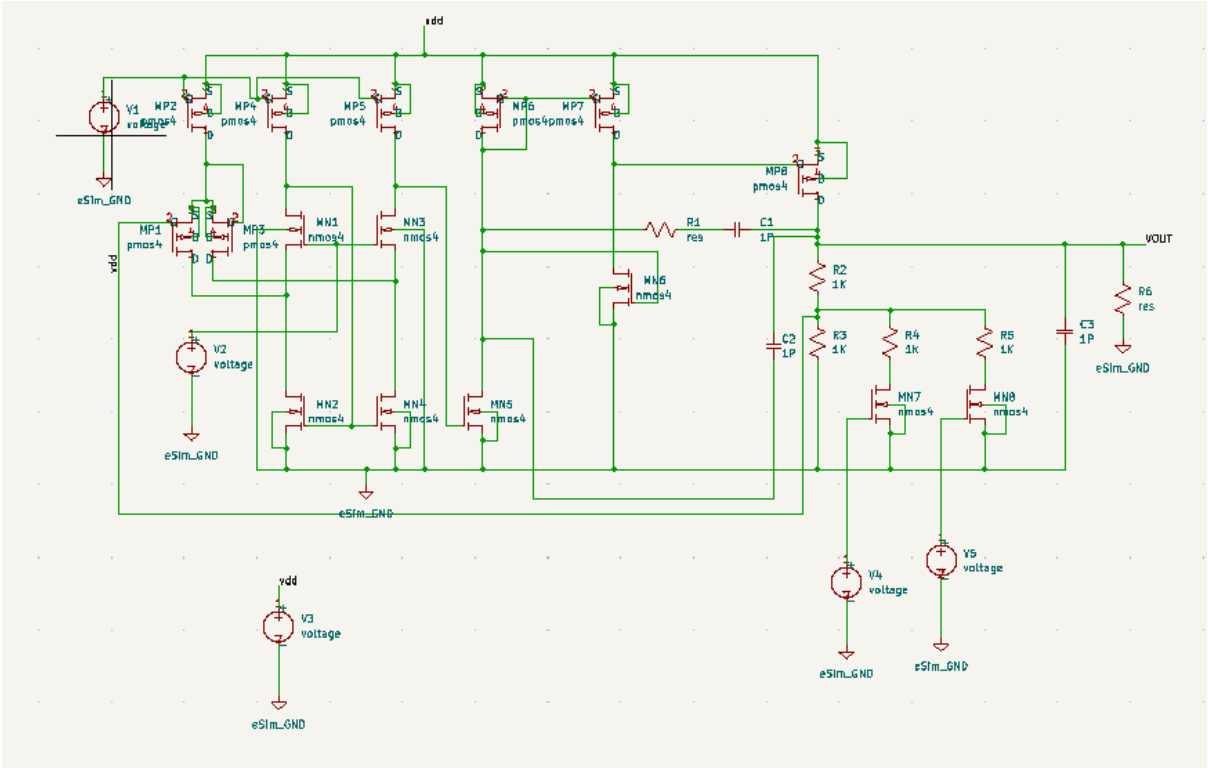


Fig 3. Programmable Low Drop-Out Voltage Regulator

Implemented Circuit Diagram :



Expected Results (Input, Output waveforms and/or Multimeter readings) : The output should exhibit a stable DC level with minimal ripple under steady-state conditions. During transient operation, such as startup or load changes, the response is expected to be smooth without significant overshoot or oscillations

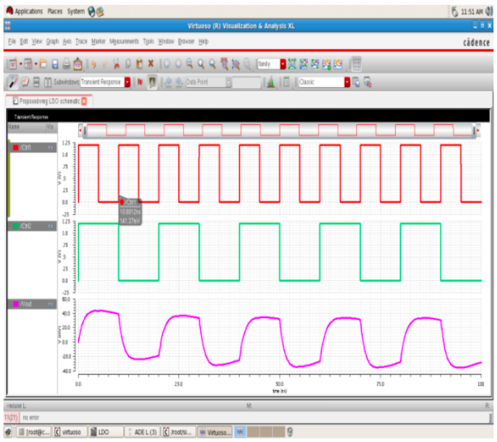
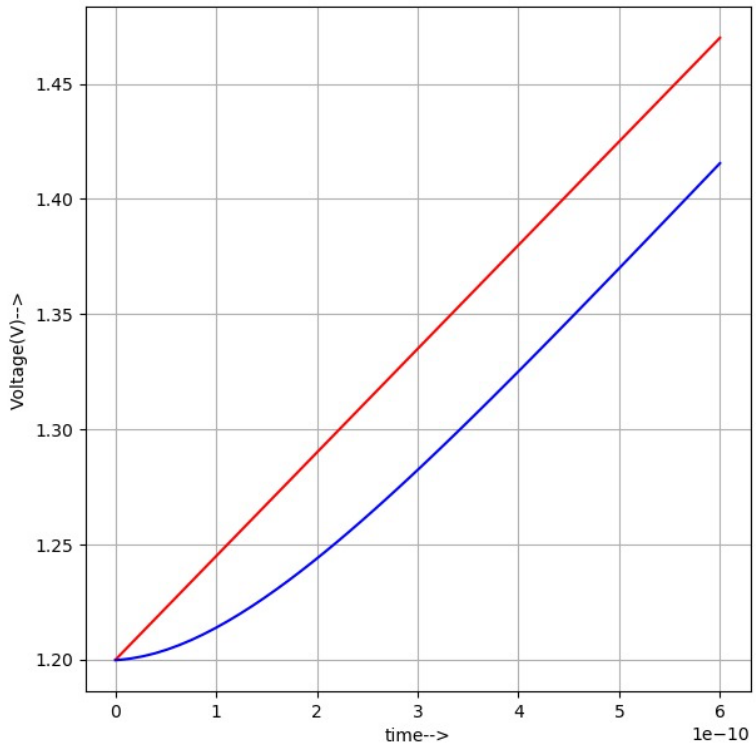


Fig 6. Proposed LDO Regulator Output

Result on eSim:



A ramp input signal was applied to evaluate the bounded-input bounded-output (BIBO) stability of the system. By varying the load, the output voltage drop can be controlled and tuned based on design requirements.

Red → Input , Blue→ Output

Research Paper/Journal/etc. :

Title : Design Analysis of Low Drop-Out Voltage Regulator with Current Buffer Compensation

Author : Rashmi Bawankar et al.

Link : https://www.ijcaonline.org/archives/volume141/number2/bawankar-2016-ijca-909558.pdf

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