Design and Simulation of Sayem Gate Using CMOS Technology in VLSI Systems

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Abstract

The reversible Sayem gate, a novel addition to VLSI systems, plays a critical role in addressing the growing demand for energy-efficient and low-power designs in modern technology. With applications in quantum computing, cryptography, and nanotechnology, reversible logic has emerged as a key area of research. This paper presents the design and simulation of the Sayem gate using CMOS technology, leveraging the capabilities of eSim software. The Ngspice simulation results confirm the accuracy and reliability of the proposed design, delivering the expected logical outputs. This study provides a comprehensive overview of the Sayem gate's architecture, its significance in current technological advancements, and its successful implementation. The results demonstrate the potential of the Sayem gate to contribute significantly to the development of sustainable and efficient VLSI systems.

Keywords: Sayem gate, novel reversible gate, eSim software, NgSpice simulation

1.Introduction

Sayem gate (SG) is a 4x4 reversible gate. The input and output vector of this gate is, I(A, B, C, D) and O (A, A'B EXOR AC, A'B EXOR AC EXOR D, AB EXOR A'C EXOR D). The Sayem gate can be used to build reversible standard sequential circuits like T flip-flop, D flip-flop along with Feynman gate. The corresponding implementation of Sayem gate has been shown in Figure 1.a. This implementation works suitable for both forward as well as backward computations, i.e., completely reversible and can be verified from the output wave forms.

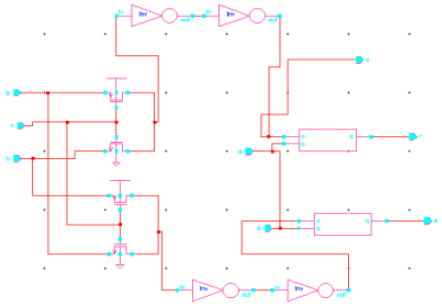


Figure 1 Sayem gate a). Schematic Diagram

2. Purpose of Sayem Gate

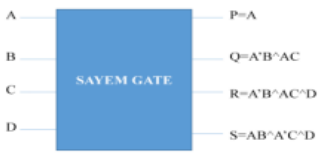
Sayem gate, the novel reversible gate, is used in various applications due to its unique characteristics. It is known for its

Energy Efficiency: Reduces power dissipation by ensuring lossless computation through reversible logic, aligning with Landauer's principle.

Information Preservation: Maintains a one-to-one mapping between input and output states, preventing information loss during computation.

Advancement in Quantum Computing: Serves as a foundational component for quantum circuits, where reversibility is essential.

3.Proposed Circuit



A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	1
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	1
0	1	1	1	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	1
1	0	1	0	1	1	1	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	0
1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	0

Figure 3.a. Block diagram of Sayem Gate,
3.b. Truth Table of Sayem Gate

Figure 3.a. shows the block diagram of the Sayem gate with three inputs and its corresponding four outputs with special logic functions. The output of the gate with respect to the input can be easily retrieved and verified using its truth table shown in Figure 3.b.

4. Schematic Diagram

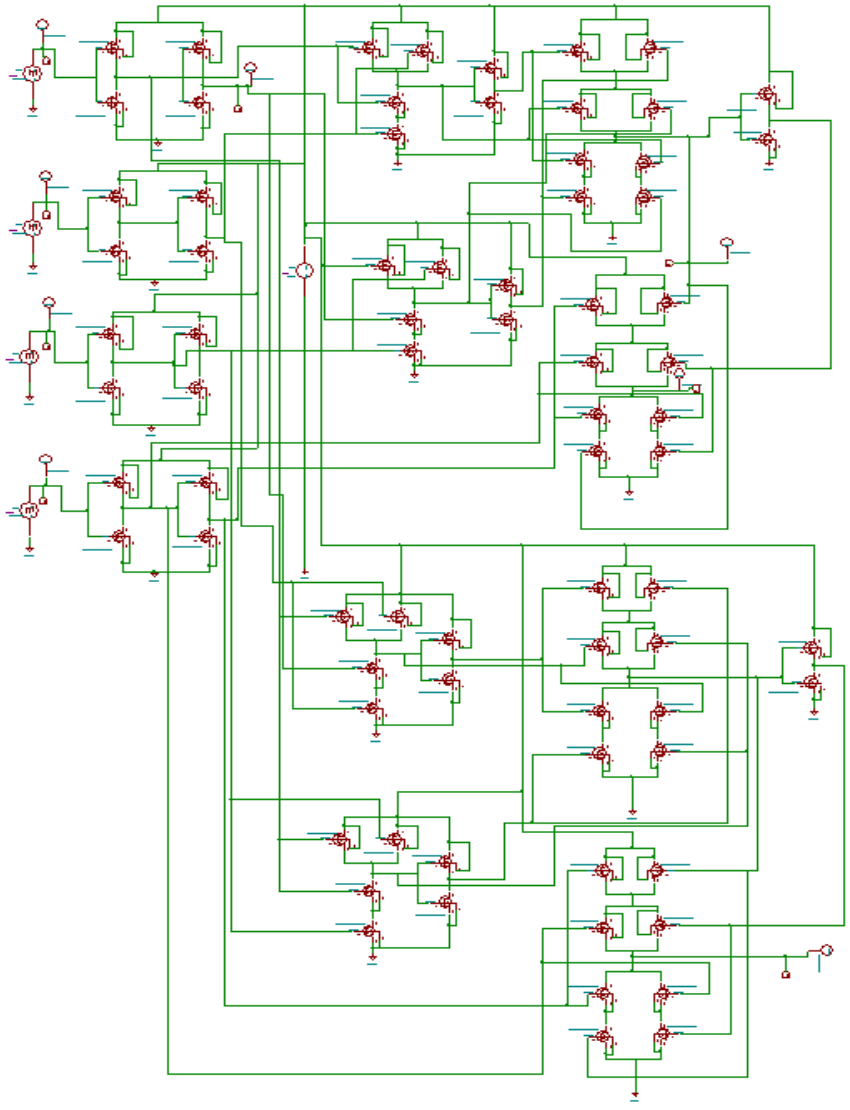


Fig 4.a. Schematic diagram of Sayem Gate using CMOS

5. NgSpice Simulation

5.a. Transient Analysis:

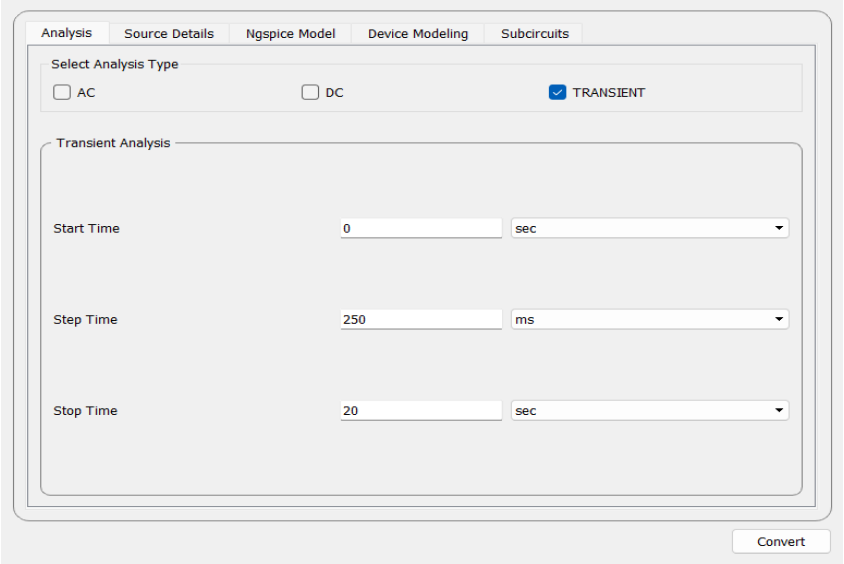


Figure 5.a. Transient Analysis of Sayem gate

5.b. Source Details:

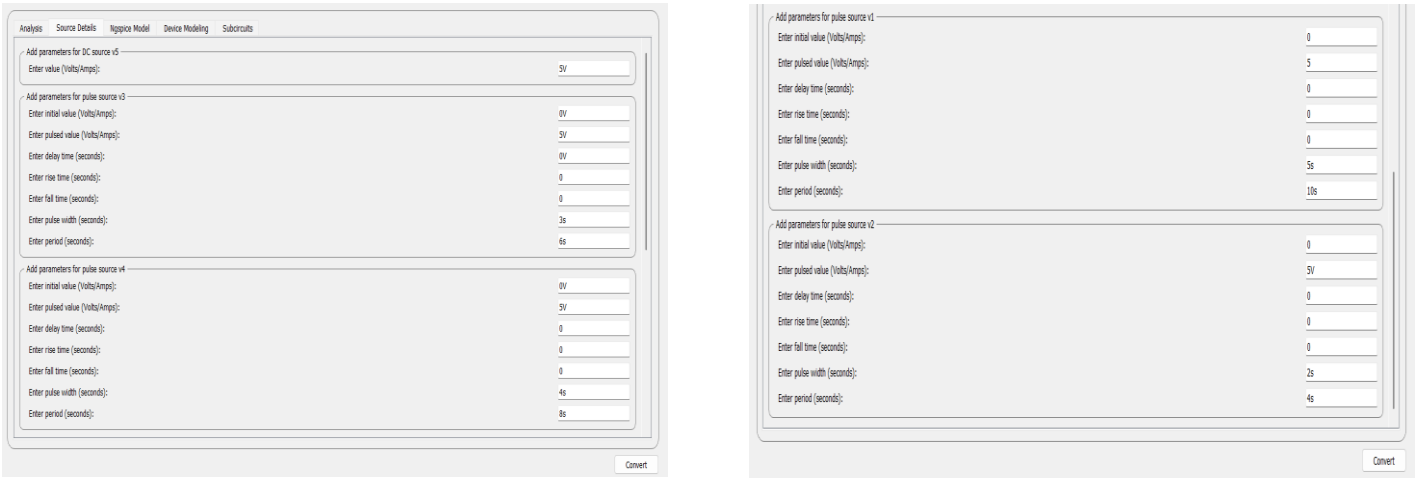


Figure 5.b. Source details of one biasing voltage and four input pulses with different clock pulses.

5.c Device Modeling:

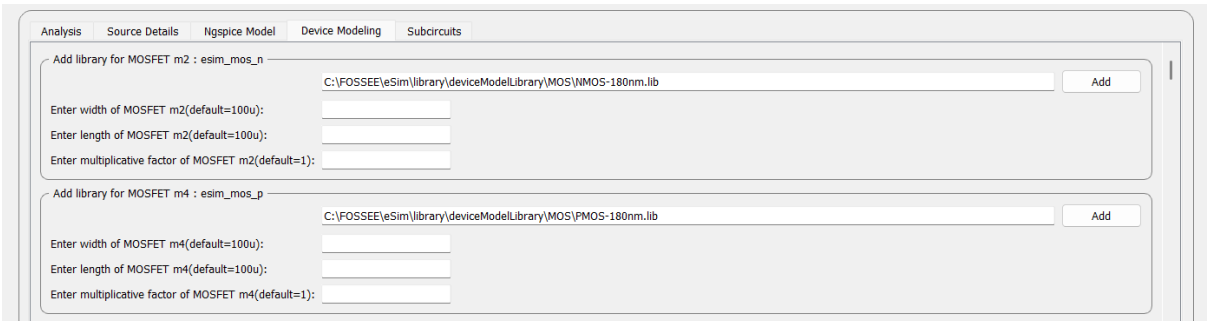
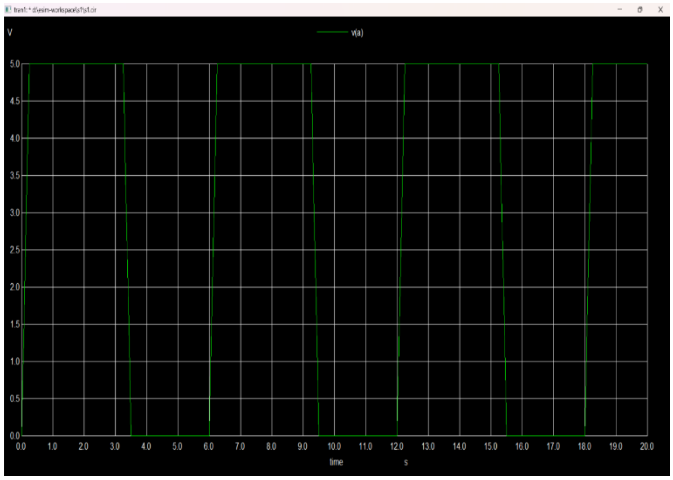


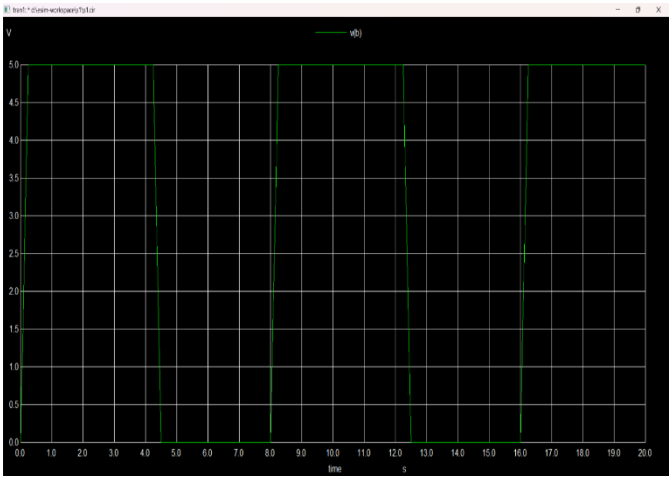
Figure 5.c. Device Modeling of PMOS and CMOS circuits used here

The width and length of the eSim NMOS and PMOS are set to be default, and the library file is added with the NMOS and PMOS 180nm program files.

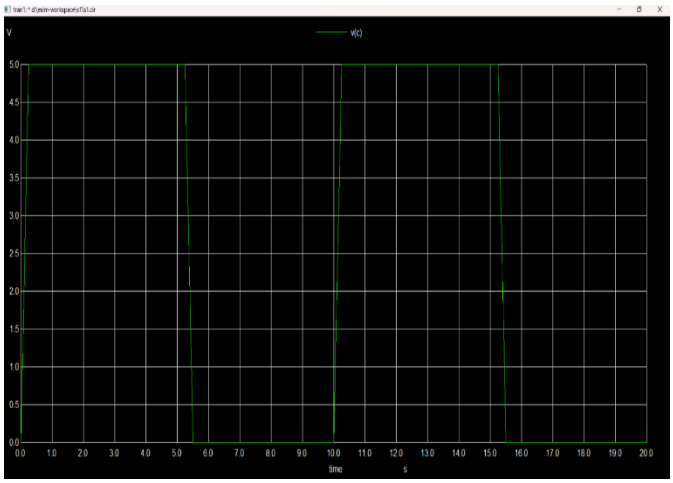
5.d. Input Waveforms



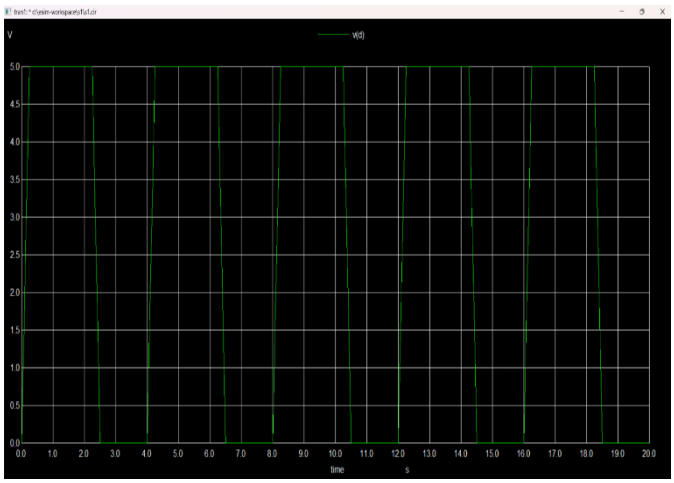
(a)



(b)



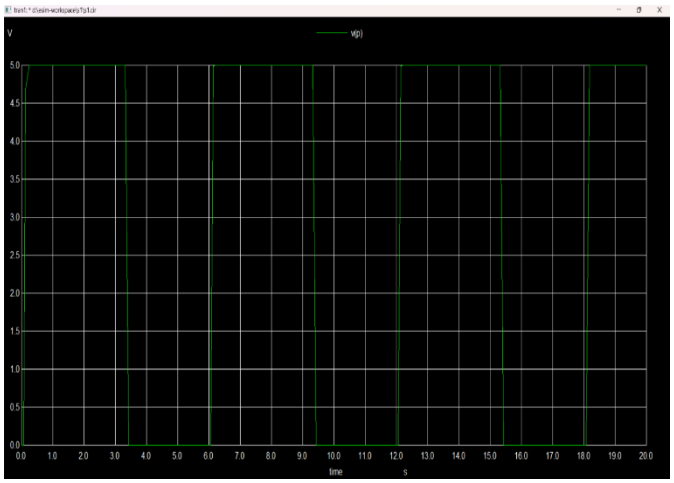
(c)

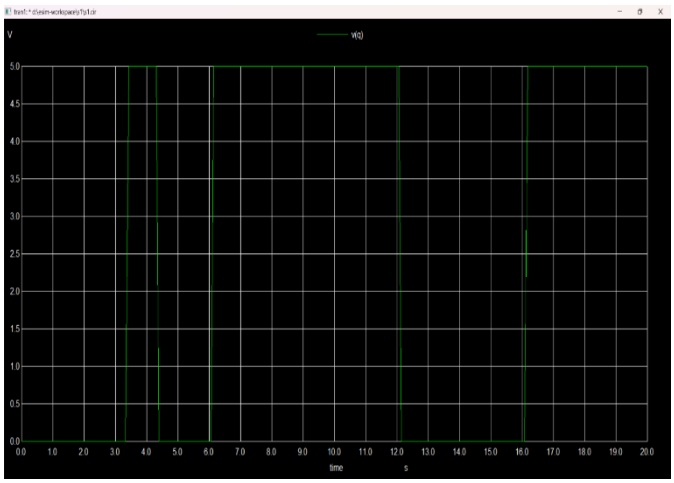


(d)

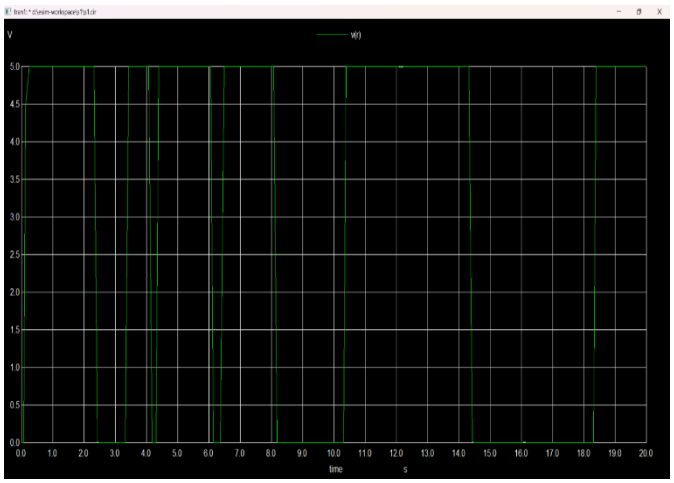
Figure 5.d. (a), (b), (c), (d) Input waveforms for the input pulses

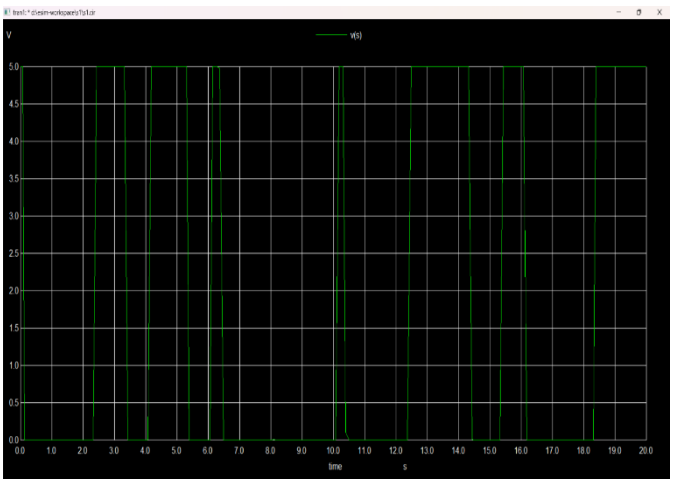
5.e. Output Waveforms





(a) (b)



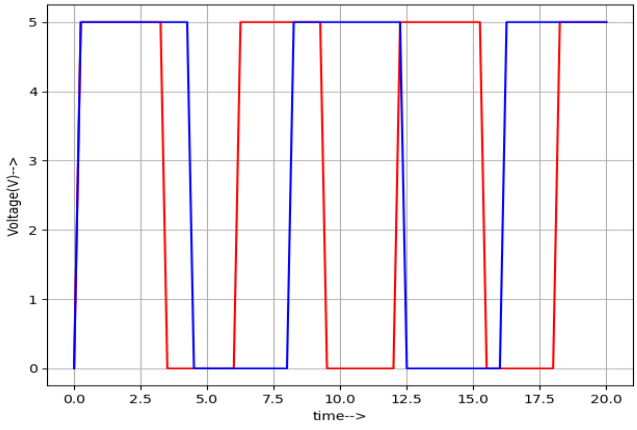


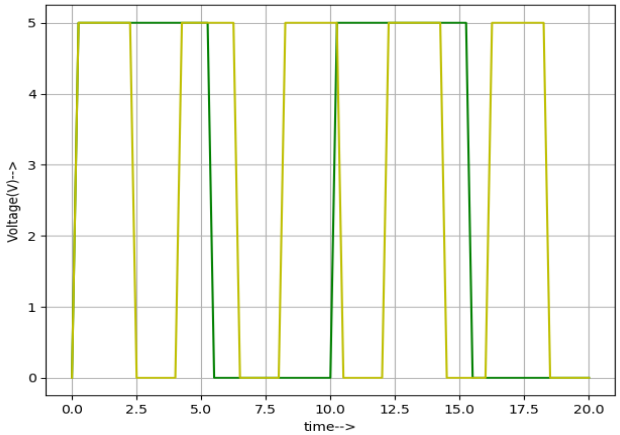
(c) (d)

Figure 5.e. (a), (b), (c), (d) 4 Output waveforms of the Sayem gate in NgSpice simulation

6. Python Plot

6.a. Input Waveforms

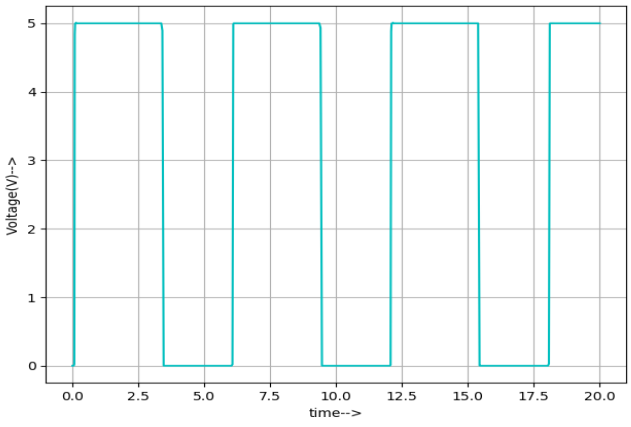


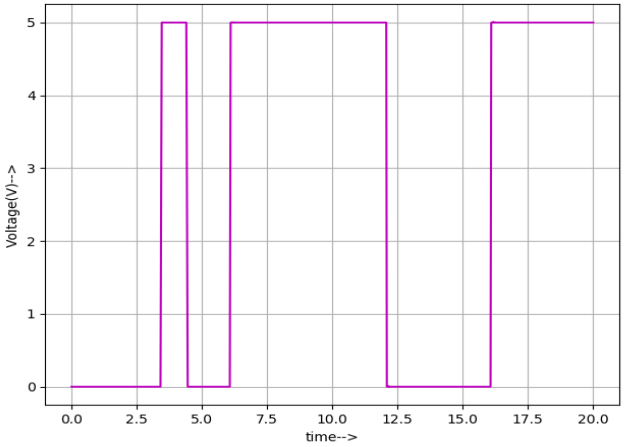


(a) **(b)**

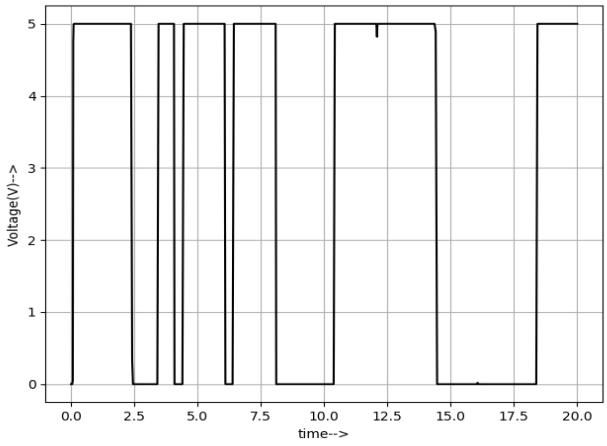
Figure 6.a (a), (b) Input Waveforms for the input pulses in Python MatPlot

6.b. Output Waveforms

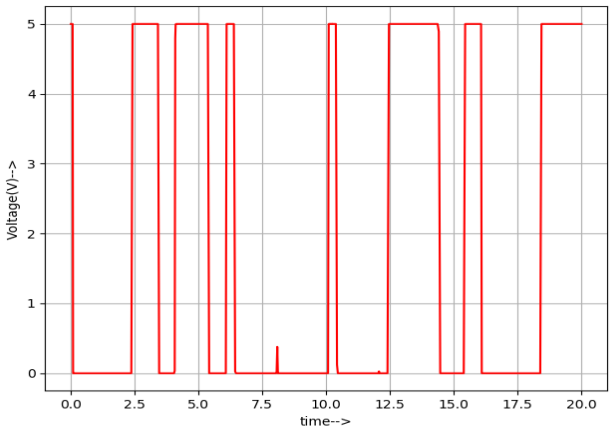




(a) (b)



(c)



(d)

Figure 6.b. (a), (b), (c), (d) 4 Output waveforms for the Sayem gate in Python MatPlot

7. Conclusion

The Sayem gate was successfully designed and simulated using CMOS technology in the eSim platform. The functionality was validated through NgSpice waveforms, and the outputs were further visualized and confirmed using Python's Matplotlib. The results aligned with the expected logical behaviour, demonstrating the accuracy and reliability of the gate. This study establishes the Sayem gate as a promising component for low-power and energy-efficient designs in modern VLSI systems, showcasing its potential for practical applications in reversible logic circuits.

8. References

Publications:

1.Title : Design and Optimization of Asynchronous counter using Reversible Logic

Author : Mr Harish k, Mrs. Chinmaye R, RVCE, Bengaluru

Volume : Vol. 4 Issue 06, June-2015

Reference link: https://www.ijert.org/research/design-and-optimization-of-asynchronous-counter-using-reversible-logic-IJERTV4IS060242.pdf

2.Title : Introduction to Reversible Logic Gates & its application

Author : Prashant. R.Yelekar (M.Tech) ,Prof. Sujata S. Chiwande Lecturer YCCE, Nagpur

Page : 7

Reference link: https://ieeexplore.ieee.org/document/9036799

3. Title **:** A Review of Reversible Gates and its Application in Logic Design

Author **:** Shefali Mamataj 1, Dibya Saha 2, Nahida Banu3

Volume **:** Volume-03, Issue-04, pp-151-161

Reference link: https://ajer.org/papers/v3(4)/T034151161.pdf