Title:

Study and Analysis of JK Master–Slave Flip-Flop for Elimination of Race-Around Condition

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Theory / Description:

The **JK master–slave flip-flop** is a sequential logic circuit designed to overcome the **race-around condition** that occurs in a conventional level-triggered JK flip-flop.

In a normal JK flip-flop, when **J = K = 1** and the clock pulse width is greater than the propagation delay of the flip-flop, the output continuously toggles between logic HIGH and logic LOW as long as the clock remains active. This repeated toggling within a single clock pulse is known as the **race-around condition**.

The master–slave configuration eliminates this issue by using **two latches connected in cascade**:

- **Master latch**
- **Slave latch**

The **master latch** is enabled during the **HIGH clock pulse**, while the **slave latch** is disabled.

When the clock goes **LOW**, the master latch is disabled and the slave latch becomes enabled, transferring the stored data to the output.

This ensures that the output changes **only once per clock cycle**, thereby eliminating multiple toggles and preventing race-around.

The output equation remains:

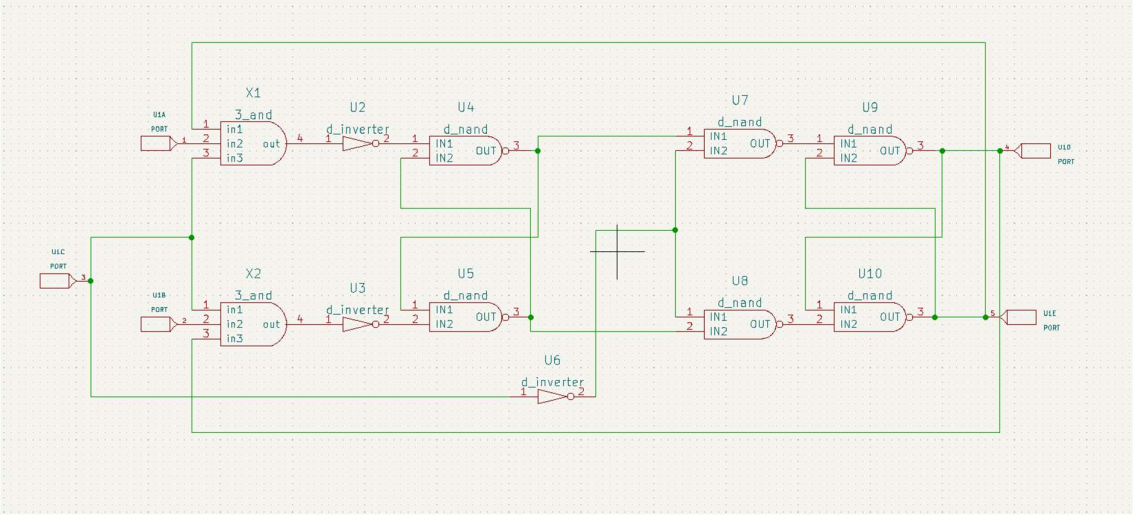
$$Q_{n+1} = J\bar{Q_n} + \bar{K}Q_n$$

This design is widely used in:

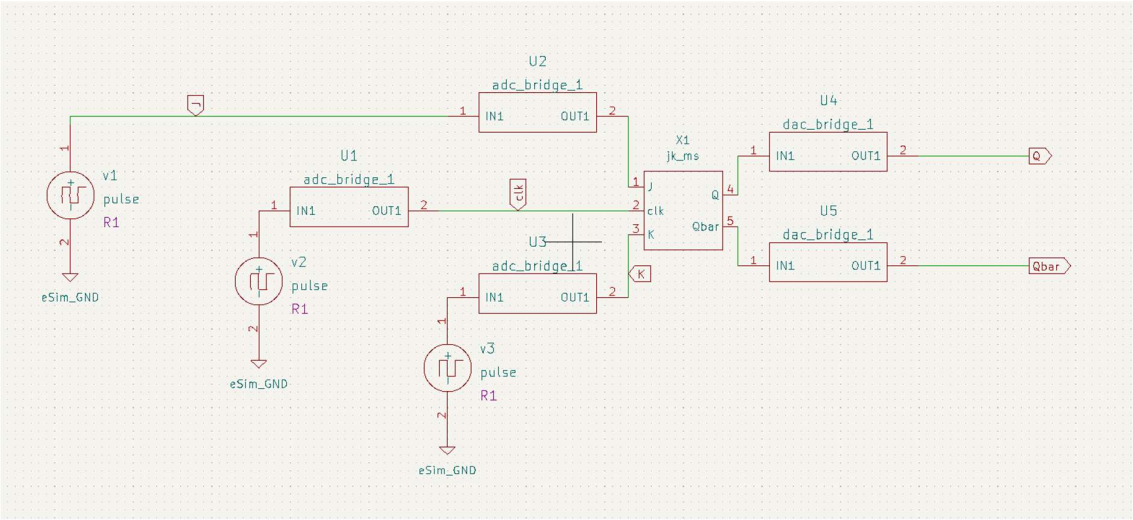
- synchronous counters
- frequency dividers
- memory registers
- digital sequential systems

Circuit Diagram:

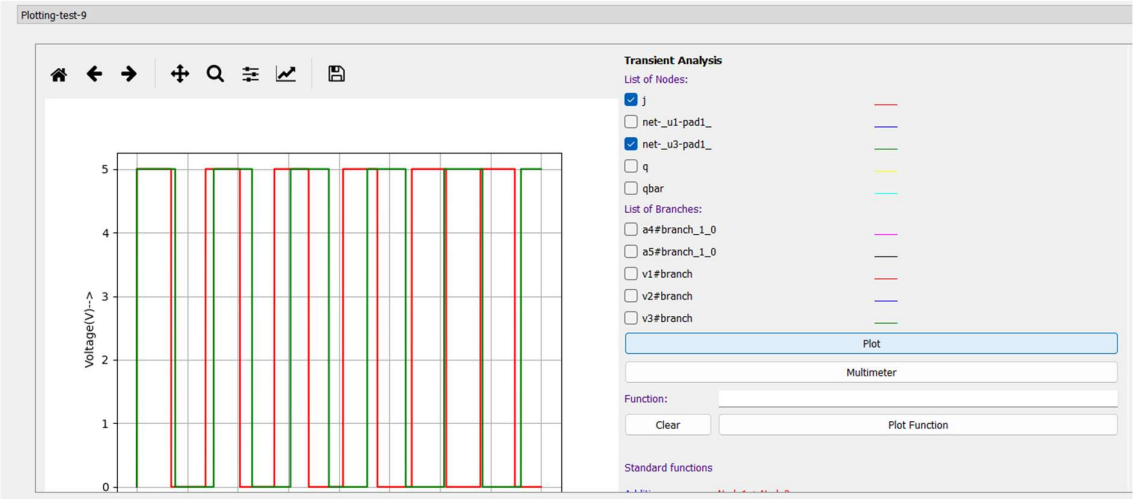
JK_master_slave schematic circuit:



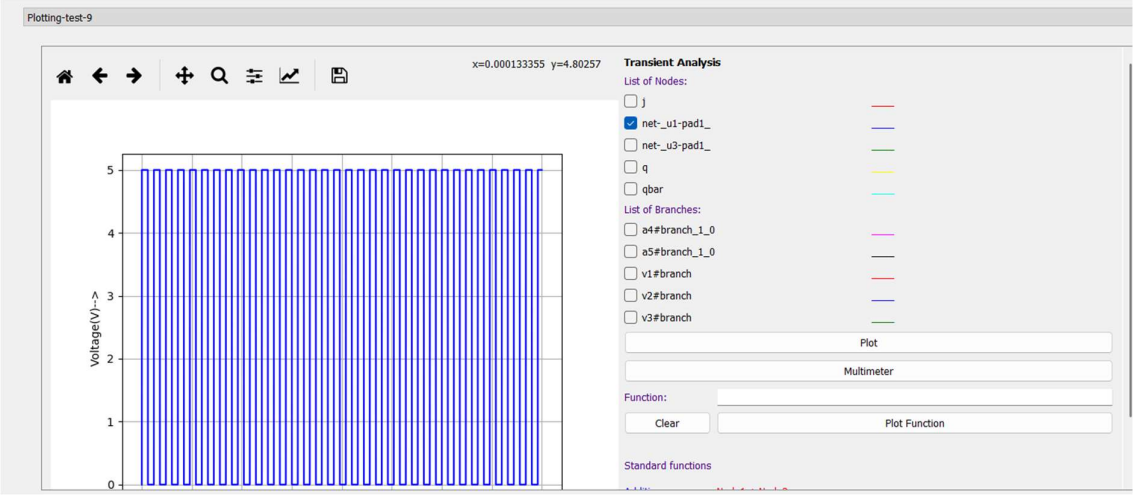
Test circuit:



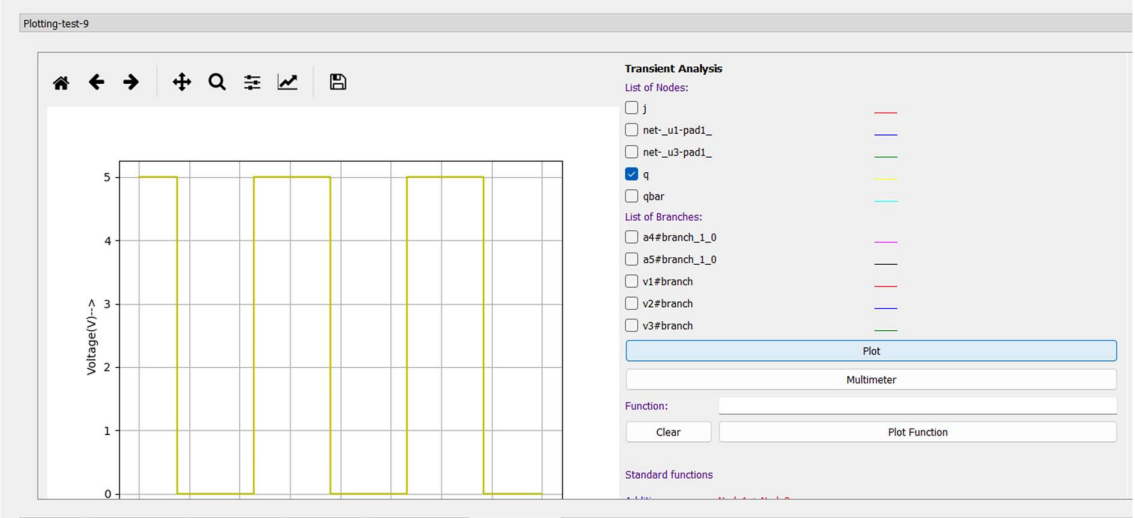
Results / Output: Input J and Input K:



Input Clock:



Output Q:



References:

1) **Title : Master-Slave JK Flip Flop**

Author : Geeks for Geeks.

Link : (Direct link to IEEE / Scopus / Google Scholar / Patent source)

2) Book : Digital Design by M. Morris

Page no.: 211 (Master Slave flipflop)

Link: https://www.mpgcamb.com/wp-content/uploads/2024/12/M.-Morris-Mano-Digital-Design-Prentice-Hall-1995.pdf