Research Migration Project

https://esim.fossee.in/research-migration-project

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Title of the circuit : Design and implementation of 4-bit binary weighted current steering DAC

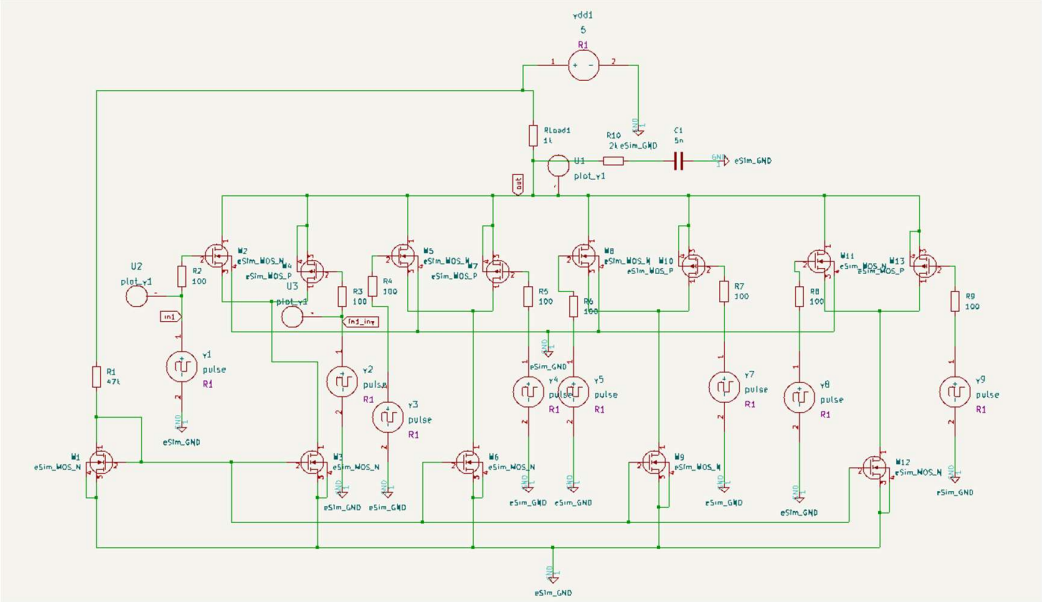
Description : This project focuses on the design and simulation of a 4-bit binary weighted current steering Digital-to-Analog Converter (DAC) using CMOS technology in the eSim environment. The DAC operates by generating binary-weighted currents (I, 2I, 4I, 8I) using NMOS current mirrors and steering them to the output node through transmission gates controlled by digital input signals. The summed current at the output is converted into a corresponding voltage using a load resistor, resulting in a staircase waveform that represents the digital-to-analog conversion.

The simulation results validate the correct operation of the DAC by producing the expected step-like output corresponding to input combinations. Minor glitches observed during switching transitions are due to inherent characteristics of binary weighted current steering DACs and have been reduced using RC filtering. The design demonstrates efficient and high-speed conversion suitable for basic VLSI.

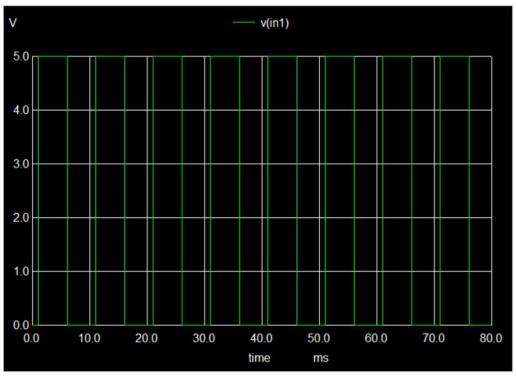
Expected Outcome: When the 4-bit binary weighted current steering DAC is simulated, it is expected to convert digital input combinations into a corresponding analog output in the form of a staircase waveform. As the digital inputs change sequentially from 0000 to 1111, the output current increases in discrete steps based on the binary-weighted contributions (I, 2I, 4I, 8I) of each branch. This current is converted into a voltage across the load resistor, producing a step-like analog output that reflects the input code. The waveform should show uniform step increments, indicating proper current scaling and correct switching operation of the transmission gates.

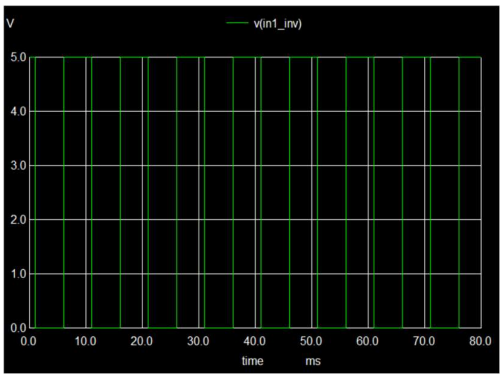
The circuit performance can be validated by observing the linearity and consistency of the output steps in the transient simulation. The presence of 16 distinct levels confirms correct 4-bit operation. Minor glitches may appear during switching transitions due to simultaneous changes in multiple bits, which is inherent to binary-weighted DACs. These effects can be reduced using filtering techniques.

Circuit Diagram :

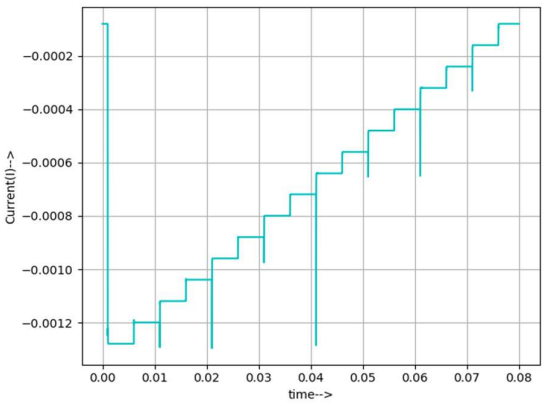


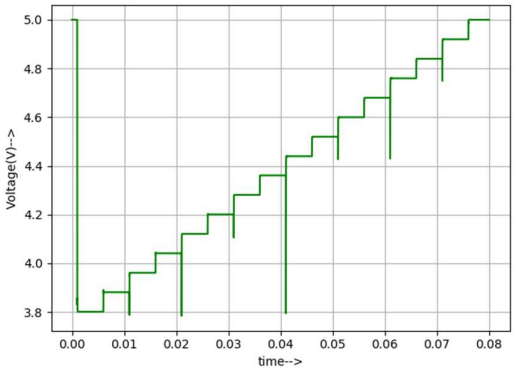
Expected Results (Input, Output waveforms) :





Note: Similar pulse waveforms are applied for V2–V2′, V3–V3′, and V4–V4′, with their periods scaled accordingly (each having twice the period of the previous signal) to ensure proper binary-weighted switching**.**





Technical Article / Journal:

Title : The Current-Steering DAC

Author : Behzad Razavi

Link : https://www.seas.ucla.edu/brweb/papers/Journals/BRWinter18DAC.pdf

References :

https://spie.org/samples/TT97.pdf

file:///C:/Users/Bharath%20Kumar/Downloads/22576-44990-1-PB.pdf

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