Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit : Design and Simulation of Cascaded hybrid amplifier using CS-CE Amplifier to gain high voltage Gain.

Theory/Description :

A hybrid cascade amplifier combines a MOSFET-based **Common Source (CS)** stage with a BJT-based **Common Emitter (CE)** stage to achieve **high voltage gain**.

The CS stage (using MOSFET) offers **high input impedance**, while the CE stage (using BJT) provides **high voltage gain**. When cascaded, the overall gain becomes the product of individual stage gains, resulting in a significantly amplified output signal.

Both stages are AC coupled via capacitors C1, C2, C3 to block DC while passing AC signals. Total voltage gain = Av1 × Av2 .

The circuit employs a **two-stage cascaded topology**, where the output of the CS amplifier is capacitively coupled to the input of the CE amplifier. Proper biasing techniques and component selection are used to ensure that both transistors operate in their respective active regions. The design avoids signal distortion while maximizing gain through optimized resistor values and bypass capacitors.

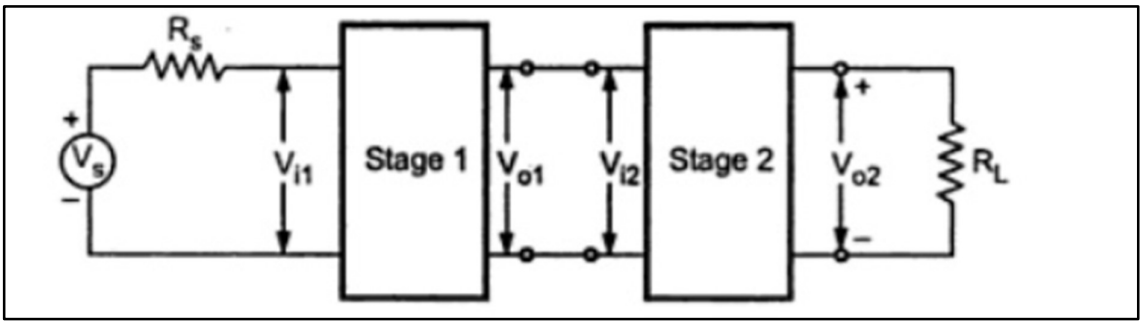

Fig 1: Two stage Cascade Amplifier

The system demonstrates **high voltage gain performance**, validated through AC analysis and frequency response simulations. The results highlight a stable midband gain and expected roll-off characteristics at low and high frequencies due to coupling and parasitic effects. The simulation confirms that cascading amplifier stages significantly enhances overall gain, making the design suitable for applications in audio amplification, communication systems, and signal processing circuits.

Reason to reproduce with eSim :

The designed cascaded hybrid amplifier using a Common Source (CS) and Common Emitter (CE) configuration is well suited for simulation and reproduction using **eSim** due to its open-source nature and integration of powerful tools such as **Ngspice** and **KiCad**. eSim provides a accessible platform for circuit design, enabling students and researchers to perform detailed analysis without the need for expensive proprietary software.

Compared to traditional manual calculations, simulation in eSim improves accuracy, reduces design time, and enables easy modification and optimization of circuit parameters. Hence, the proposed amplifier circuit is highly suitable for reproduction and validation using eSim.

Simulation Note

AC sweep analysis has been used to evaluate the performance of the amplifier, and the results are shown in the file **Testing.cir.out**.

To simulate the project:

1. Extract the provided ZIP file.
2. Open **eSim**.
3. Load the **Testing** project folder (which contains the .proj file).
4. Run the simulation to reproduce the results.

Expected Outcome/outputs :

Upon simulation of the cascaded hybrid amplifier (CS-CE configuration) using eSim, the circuit is expected to exhibit significant voltage amplification due to the combined effect of the Common Source (MOSFET) and Common Emitter (BJT) stages.

1. Input: Sinusoidal signal of 0.5mV amplitude at 1kHz

2. Output: Amplified sinusoidal signal with: - **Voltage gain ≈ 150 (simulated) or 43.52 dB.**

3. Frequency response: Maximum gain occurs in the **mid-band region.**

Circuit Diagram(s) :

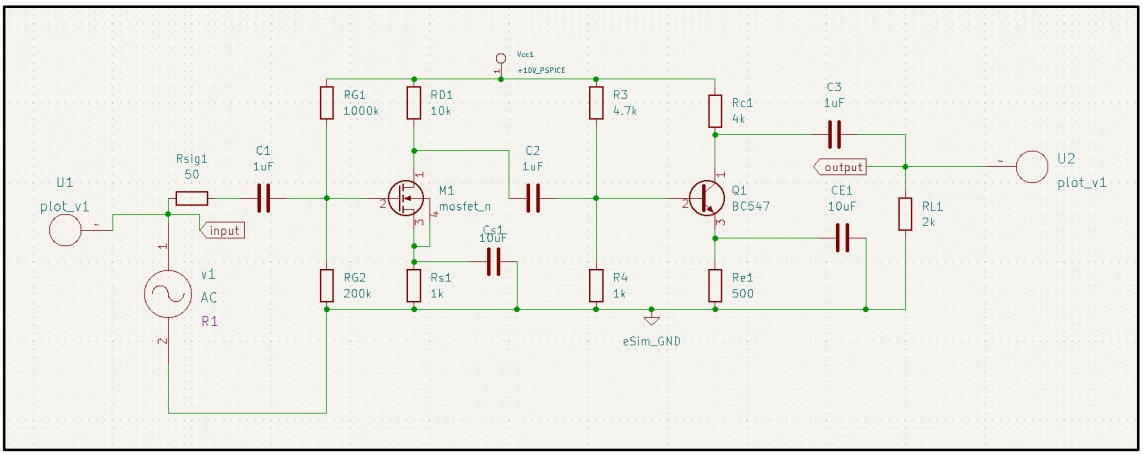

Fig 2: Circuit diagram of the cascaded hybrid amplifier (CS-CE config) using eSim

Block Diagram (s) :

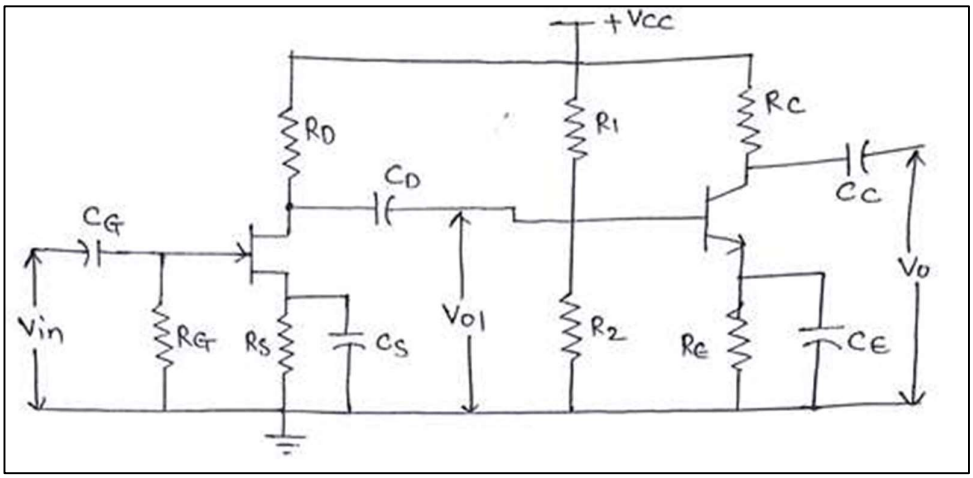

Fig 3: Simplified circuit diagram.

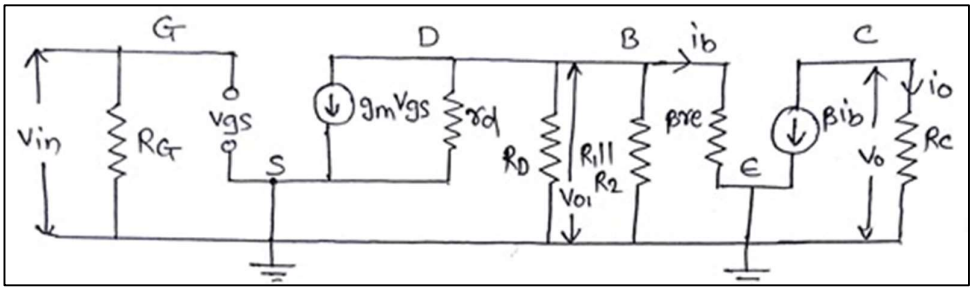

Fig 4: AC equivalent Small Signal Model diagram.

Expected Results (Input, Output waveforms and/or Multimeter readings) :

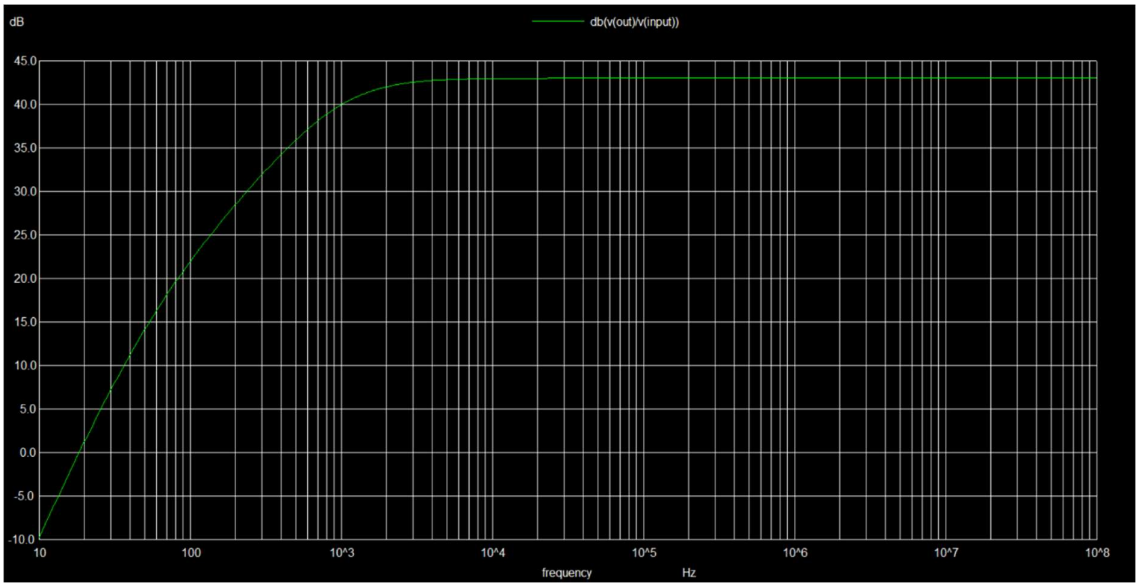

Fig 5: AC Sweep Analysis (43dB)

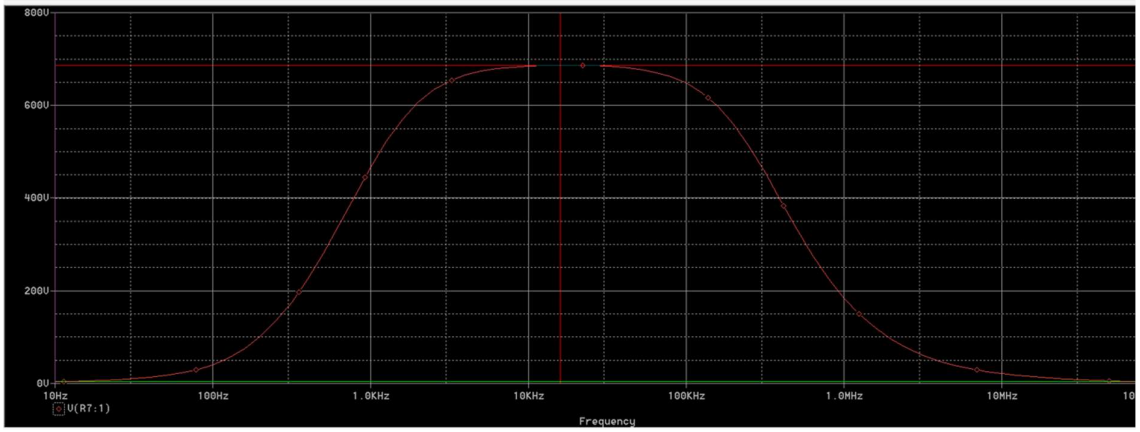

Fig 6: Ac sweep Analysis on Pspice.

Simulation Results and Output Analysis

Voltage Gain (Time-Domain Analysis)

From Transient Analysis.

→ I/P Signal Amplitude : 2 mV.

→ Output Signal Amplitude : 300 mV.

$$A_V = \frac{V_o}{V_i} \Rightarrow \frac{300\ mV}{2\ mV} \approx 150$$

$$A_V\ dB \rightarrow 20 \log(150) \Rightarrow 43.25\ dB$$

Hence, the voltage gain ≈ 150 and 43.25 dB

Need of cascading amplifiers:

- Cascading amplifiers are used to increase signal strength in Television receiver.
- In the cascading amplifier output of first stage is connected to input of second stage. A single stage amplifier is not sufficient to build a practical electronic system.
- Although the gain of amplifier depends on device parameters and circuit components, there exists upper limit for gain to be obtained from single stage amplifier. Hence, the gain of single stage amplifier is not sufficient in practical application.
- To overcome this problem, we need to cascade two or more stage of amplifier to increase overall voltage gain of amplifier. When more than one stages used in succession it is know as multi-stage amplifier.
- The disadvantage is bandwidth decrease as number of stages increases

Conclusion

The hybrid CS-CE amplifier was successfully designed and simulated using eSim/ngspice. The circuit combines a common-source MOSFET stage with a common-emitter BJT stage to achieve high overall amplification.

The simulation results show that the amplifier provides a voltage gain of approximately 150, which corresponds to a midband gain of about 43 dB. The frequency response demonstrates a stable midband region, with expected attenuation at low and high frequencies due to coupling capacitors and device limitations.

The transient analysis confirms that the output waveform is an amplified version of the input signal with acceptable linearity, indicating proper biasing and operation in the active region.

Overall, the design validates that multistage amplification using MOSFET and BJT stages is effective in achieving significant gain while maintaining signal integrity.

Research Paper/Journal/etc. :

"The proposed CS–CE cascaded amplifier follows the same principle of multistage amplification as discussed in the referenced work, where cascading amplifier stages significantly improves overall voltage gain and performance."

Title : Design of Cascaded Common Source Low Noise Amplifier for S-Band using Transconductance Feedback
Author : Anu Ravindran, Karthigha Balamurugan, M. Jayakumar

Page No. : Vol. 9, Issue 16, Pages 1–7 (2016)

Link : https://indjst.org/articles/design-of-cascaded-common-source-low-noise-amplifier-for-s-band-using-transconductance-feedback

Source/Reference(s) :

1. Sedra & Smith, Microelectronic Circuits, Oxford University Press.

2. Razavi, Design of Analog CMOS Integrated Circuits.

3. https://ngspice.sourceforge.io/

4. https://esim.fossee.in/

5. IEEE journals and conferences on Multistage Amplifiers
