Design and Simulation of a VCO-Based Analog-to-Digital Converter Using Time-Domain Conversion

A Project Report Submitted by

Padhmanethrri S
Department of Electronics and Communication Engineering

Sri Sivasubramaniya Nadar College of Engineering
Chennai, Tamil Nadu
April 2026

Abstract

Analog-to-Digital Converters (ADCs) are essential for converting real-world analog signals into digital form for processing. This project presents the design and simulation of a Voltage-Controlled Oscillator (VCO)-based ADC using a time-domain conversion approach.

In this system, the input analog voltage is converted into a frequency using a VCO, where higher input voltage results in higher oscillation frequency. The signal is then conditioned using a buffer and passed through a sampling window to define a fixed observation interval. A 4-bit counter counts the number of pulses during this interval, and a latch captures and holds the final count, providing a stable digital output proportional to the input voltage.

The circuit is implemented and simulated using eSim, enabling integrated analysis of analog and digital components. Simulation results show a clear and consistent relationship between input voltage and digital output, confirming correct operation of the proposed ADC.

This work demonstrates a simple and efficient time-domain ADC architecture and provides insight into mixed-signal VLSI design.

TABLE OF CONTENTS

INTRODUCTION

Analog signals exist naturally in the real world in the form of sound, temperature, light, and other physical quantities, whereas most modern electronic systems operate using digital signals. Therefore, Analog-to-Digital Converters (ADCs) play a crucial role in bridging the gap between analog and digital domains by converting continuous signals into discrete digital values.

Conventional ADC architectures such as flash, successive approximation (SAR), and pipeline ADCs are widely used, but they often involve complex circuitry and may face limitations in terms of power consumption and scalability, especially in advanced CMOS technologies. To address these challenges, time-domain ADCs have emerged as an alternative approach, where the analog signal is represented using time or frequency instead of voltage.

One of the most efficient implementations of time-domain ADCs is the Voltage-Controlled Oscillator (VCO)-based ADC. In this approach, the input analog voltage controls the frequency of an oscillator, converting voltage into frequency. This frequency is then measured over a fixed time interval and translated into a digital value using counting techniques.

In this project, a VCO-based ADC is designed and simulated using the eSim platform. The system consists of a VCO, buffer stage, sampling window, digital counter, and latch. The design demonstrates the complete process of voltage-to-frequency conversion, frequency-to-digital conversion, and output stabilization, providing a simple and effective solution for analog-to-digital conversion in mixed-signal VLSI systems.

LITERATURE REVIEW

Analog-to-Digital Converters (ADCs) are fundamental components in mixed-signal systems, enabling the interface between analog real-world signals and digital processing units. Conventional ADC architectures such as flash, successive approximation (SAR), and pipeline ADCs have been widely studied and implemented due to their high speed and accuracy. However, these architectures often involve complex analog circuitry and face challenges related to power consumption, scalability, and design complexity in deep submicron CMOS technologies [3], [4].

To overcome these limitations, time-domain ADCs have emerged as an alternative approach, where the analog input signal is converted into a time or frequency parameter rather than being directly quantized in the voltage domain. This approach leverages the advantages of digital circuits, making the design more scalable and robust to process variations [1].

Among various time-based architectures, Voltage-Controlled Oscillator (VCO)-based ADCs have gained significant attention. In these systems, the input voltage controls the oscillation frequency of the VCO, effectively performing voltage-to-frequency conversion. The resulting frequency is then measured over a defined time interval and converted into a digital value using counting techniques. Studies have shown that VCO-based ADCs offer reduced circuit complexity, lower power consumption, and better compatibility with nanoscale technologies [2].

Research also highlights that VCO-based ADCs provide improved noise immunity compared to traditional voltage-domain ADCs, as the information is encoded in frequency rather than amplitude. This makes them particularly suitable for low-voltage and low-power applications. Additionally, industry reports emphasize the growing importance of time-based conversion techniques in modern integrated circuits due to their efficiency and ease of implementation [5], [6].

Despite these advantages, certain challenges exist in VCO-based ADC designs. Non-linearity in the VCO can affect the accuracy of conversion, and the resolution is often limited by the counter size and sampling duration. Various techniques, including calibration methods and advanced architectures, have been proposed in literature to improve linearity and enhance resolution [2].

In this work, a simplified VCO-based ADC is designed and simulated using the eSim platform. The objective is to demonstrate the fundamental concept of time-domain conversion and validate the relationship between input voltage and digital output through waveform analysis.

OBJECTIVE

The main objective of this project is to design and simulate a Voltage-Controlled Oscillator (VCO)-based Analog-to-Digital Converter using a time-domain conversion technique.

The specific objectives are as follows:

• To convert an analog input voltage into a corresponding frequency using a VCO.

• To implement a sampling mechanism to define a fixed observation interval for measurement.

• To design a 4-bit digital counter to count the number of pulses generated within the sampling window.

• To use a latch to capture and hold the final digital output for stable representation.

• To simulate and verify the complete system using the eSim platform.

• To analyze the relationship between input voltage and digital output through waveform observation.

SYSTEM OVERVIEW

The proposed system implements a VCO-based Analog-to-Digital Converter using a time-domain conversion approach. The design consists of a current-starved ring oscillator, a buffer stage, a sampling window, a digital counter, and latch elements.

The Voltage-Controlled Oscillator (VCO) is realized using a 3-stage current-starved ring oscillator operating at 5V. The input analog voltage controls the oscillation frequency, where higher input voltage results in higher frequency, achieving voltage-to-frequency conversion.

The oscillator output is non-ideal and is therefore passed through a buffer stage consisting of four cascaded CMOS inverters to obtain a clean square wave suitable for digital processing. Although this introduces a small delay, it significantly improves signal integrity.

A sampling window, implemented using an AND gate, controls the duration during which the oscillator pulses are allowed to pass, ensuring measurement over a fixed interval.

The gated signal is applied to a 4-bit counter using D flip-flops, which counts the number of pulses and produces a binary output corresponding to the input voltage.

Finally, latch elements capture and hold the counter output at a specific sampling instant. A small timing margin is considered to account for propagation delays, ensuring reliable data capture and a stable digital output.

Thus, the system performs analog-to-digital conversion through voltage-to-frequency conversion, pulse counting, and output stabilization.

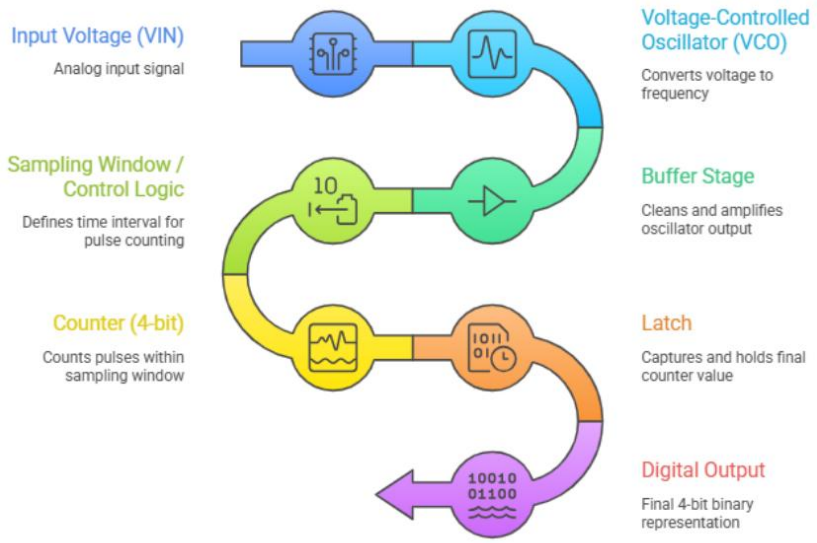

Fig. 1: Block Diagram of VCO-Based ADC

CIRCUIT DESIGN

8.1 Voltage-Controlled Oscillator (VCO)

The VCO is implemented using a 3-stage current-starved ring oscillator operating at 5V. The input voltage controls the current through the inverter stages, thereby controlling the oscillation frequency. As the input voltage increases, the delay reduces and the frequency increases, achieving voltage-to-frequency conversion.

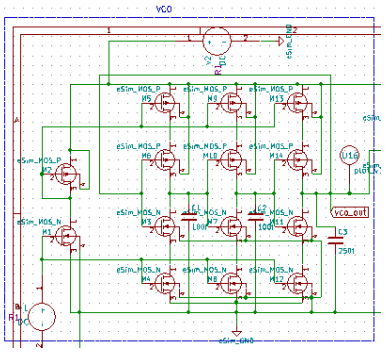

Fig. 2: Current-Starved VCO

8.2 Buffer Stage

The output of the VCO is non-ideal and does not have sharp transitions. To improve signal quality, a buffer consisting of four cascaded CMOS inverters is used. This stage converts the waveform into a clean square wave suitable for digital circuits. Although it introduces a small delay, it ensures reliable signal integrity.

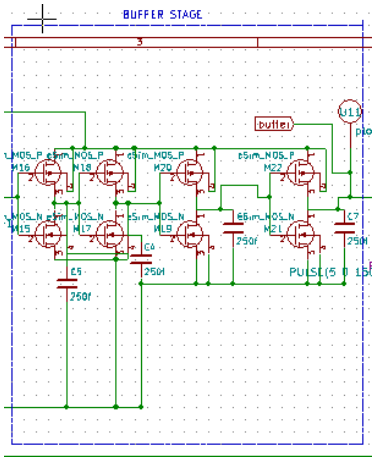

Fig. 3: Buffer using CMOS Inverters

8.3 Sampling Window

A sampling window is implemented using an AND gate. One input is the buffered oscillator signal and the other is a control pulse. This allows the signal to pass only during a fixed time interval, ensuring controlled measurement of pulses.

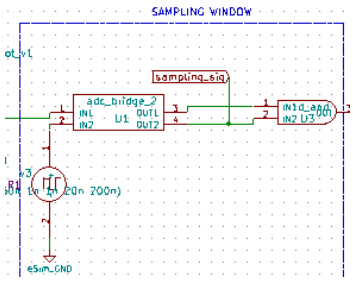

Fig. 4: Sampling Window using AND Gate

8.4 4-bit Counter

The gated signal is applied to a 4-bit counter implemented using D flip-flops. The counter increments with each incoming pulse and produces binary outputs (Q0–Q3). The count represents the number of oscillations within the sampling window.

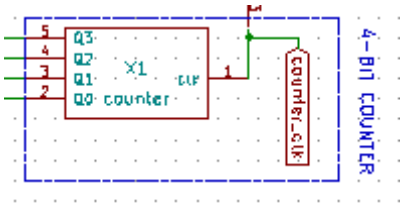

Fig. 5: 4-bit Counter

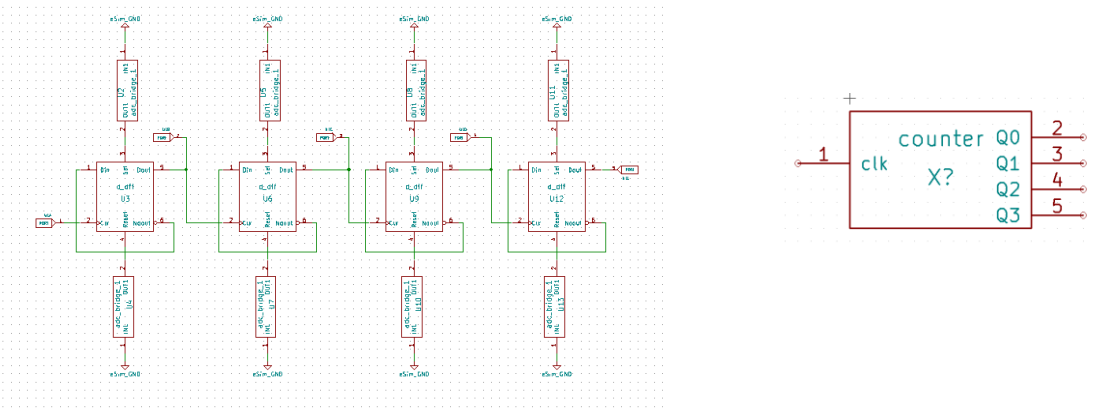

Fig. 6: Sub circuit of counter

8.5 Latch

Latch elements are used to capture and hold the counter output at a specific sampling instant. This ensures that the output remains stable and does not change continuously, providing a steady digital representation of the input voltage.

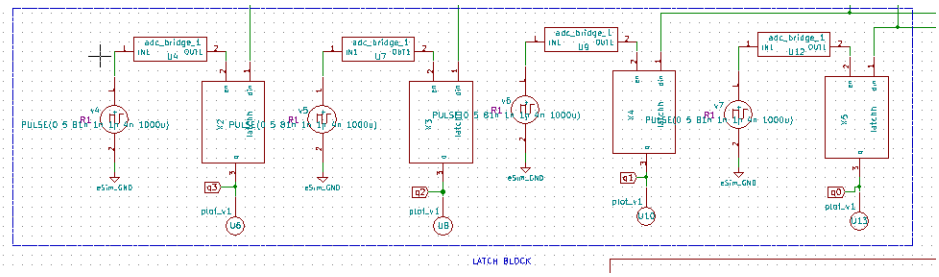

Fig. 6: Latch Circuit

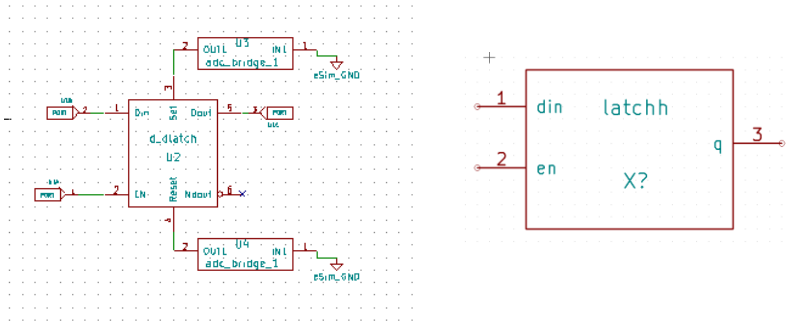

Fig. 7: Sub circuit of D-latch

WORKING PRINCIPLE

The operation of the proposed VCO-based ADC follows a sequential flow based on time-domain conversion. Initially, the input analog voltage (VIN) is applied to the VCO. As VIN increases, the oscillation frequency of the VCO increases correspondingly. The oscillator output is then passed through a buffer stage to obtain a clean square wave suitable for digital processing. This signal is allowed to pass through a sampling window for a fixed time interval. During this interval, the pulses are fed to the counter. The 4-bit counter counts the number of pulses received within the sampling window and generates a binary output (Q0–Q3). At a specific sampling instant, the latch captures the counter output and holds it constant. This latched value represents the digital equivalent of the input analog voltage. Thus, higher input voltage results in higher frequency, leading to a greater pulse count and a higher digital output.

DESIGN SPECIFICATIONS

The proposed VCO-based ADC operates with a supply voltage of 5V and accepts an input voltage range of 0V to 5V. The system is implemented using CMOS technology and simulated using the eSim platform.

The Voltage-Controlled Oscillator (VCO) is realized using a 3-stage current-starved ring oscillator. The oscillation frequency is given by:

$$f = \frac{1}{2N \cdot t_d}$$

where N=3 and td is the propagation delay of each stage. Since the delay is inversely proportional to current, and the current is controlled by the input voltage,

$$t_d \propto \frac{1}{I} \Rightarrow f \propto V_{IN}$$

Thus, the oscillation frequency increases with input voltage. The observed frequency range of operation is approximately **40 MHz to 480 MHz**.

A 4-bit asynchronous counter is used, with a maximum count given by: $2^4-1=15$

To ensure proper utilization of the counter at the maximum frequency, the required counting duration is calculated as:

$$t = \frac{15}{480 \times 10^6} \approx 31\ \text{ns}$$

Considering a startup delay of approximately 50 ns in the ring oscillator, the effective sampling instant becomes:

$$t_{sampling} = 50\ \text{ns} + 31\ \text{ns} = 81\ \text{ns}$$

This sampling instant ensures that the counter captures a meaningful digital value corresponding to the input voltage. The digital output is therefore proportional to the input voltage through frequency:

$$\text{Digital Output} \propto f \propto V_{IN}$$

SIMULATION SETUP

The proposed VCO-based ADC is simulated using the eSim platform, enabling analysis of both analog and digital circuit behavior.

The following input signals are used:

• **Analog Input Voltage (VIN):**

A DC input voltage is applied to the VCO and varied to observe system behavior. The test input values used are: **VIN = 0.7 V, 1.2 V, 2.5 V, 3 V**

These values are chosen to analyze the variation in oscillation frequency and corresponding digital output.

• **Sampling Window Signal:**

A pulse signal is used to generate the sampling window through an AND gate:

PULSE(5 0 150n 1n 1n 20n 200n)

This ensures that counting occurs only within a defined time interval.

• **Latch Enable Signal**

A pulse signal is used to trigger the latch and capture the counter output:

PULSE(0 5 81n 1n 1n 4n 1000u)

The latch is activated at approximately 81 ns, corresponding to the calculated sampling instant. Due to propagation delays in the oscillator, buffer, and logic stages, a small timing margin (80–90 ns) is considered to ensure reliable data capture.

RESULTS & WAVEFORMS

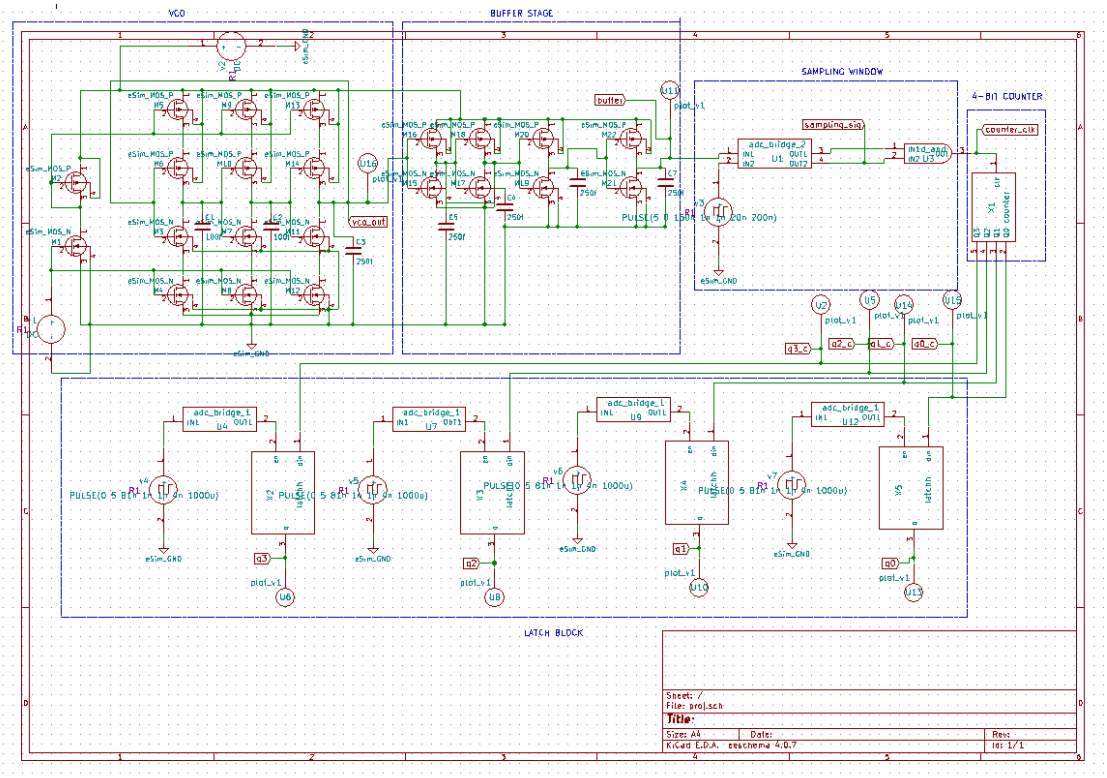

Fig. 8: Complete VCO-Based ADC Circuit in eSim

The minimum input voltage is considered as approximately 0.7 V, as this corresponds to the threshold voltage of the MOS transistors, below which the VCO does not operate effectively.

VCO OUTPUT

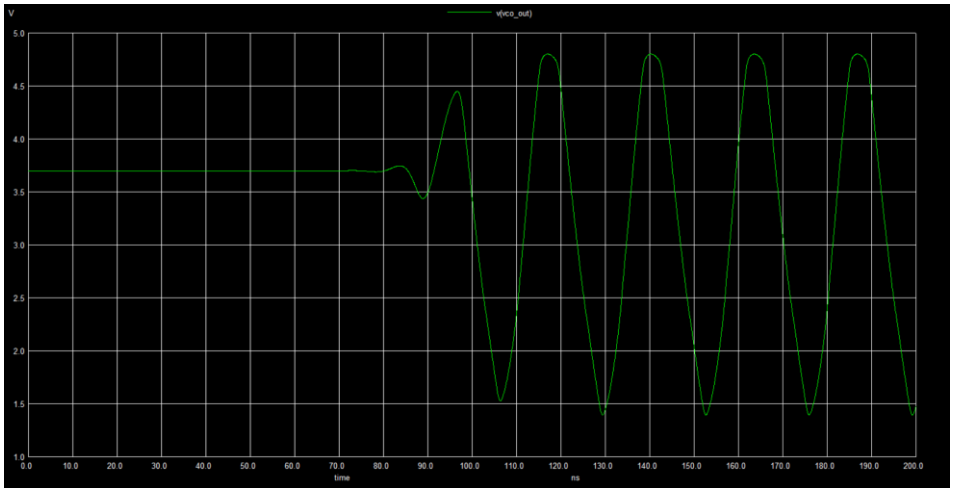

Fig. 9: VCO output when V_{in}=0.7V

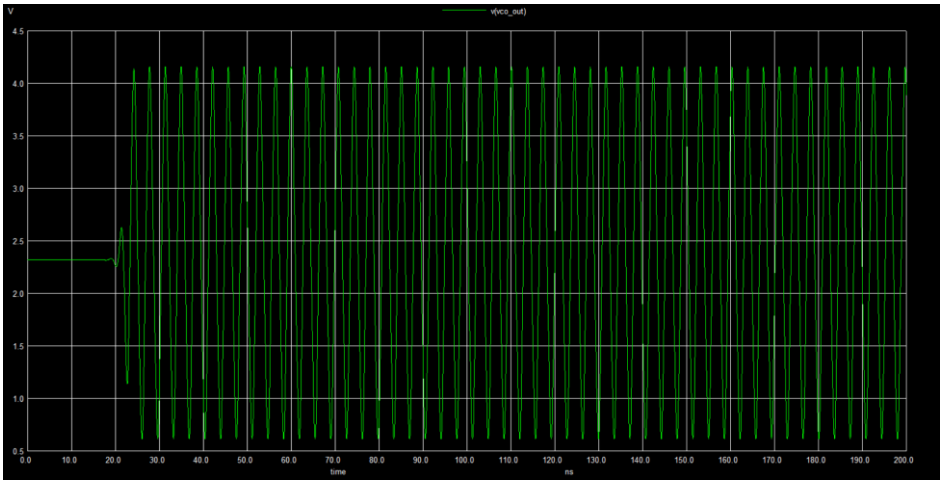

Fig. 10: VCO output when V_{in}=1.2V

The VCO output waveform shows oscillations whose frequency depends on the input voltage. For VIN = 0.7V, the oscillation frequency is relatively low, whereas for VIN = 1.2V, the frequency increases noticeably. This confirms that the oscillator frequency is directly controlled by the input voltage. The waveform is non-ideal and does not exhibit perfectly sharp transitions due to the analog nature of the current-starved ring oscillator. However, the increase in frequency with input voltage verifies correct voltage-to-frequency conversion.

BUFFER OUTPUT

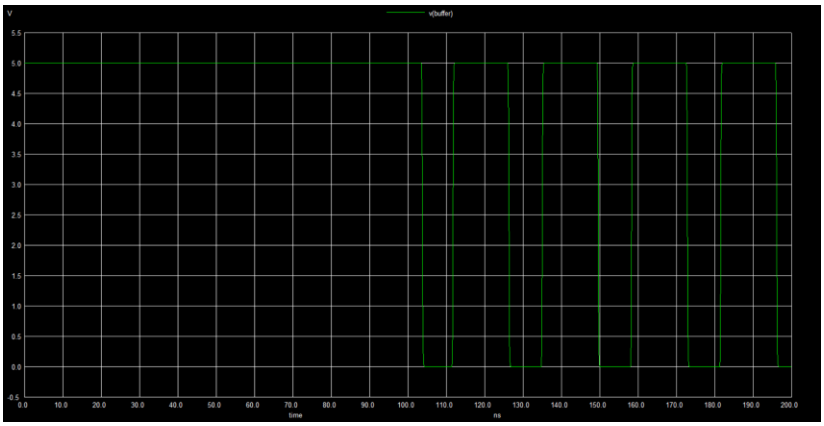

Fig. 11: Buffer output when V_{in}=0.7V

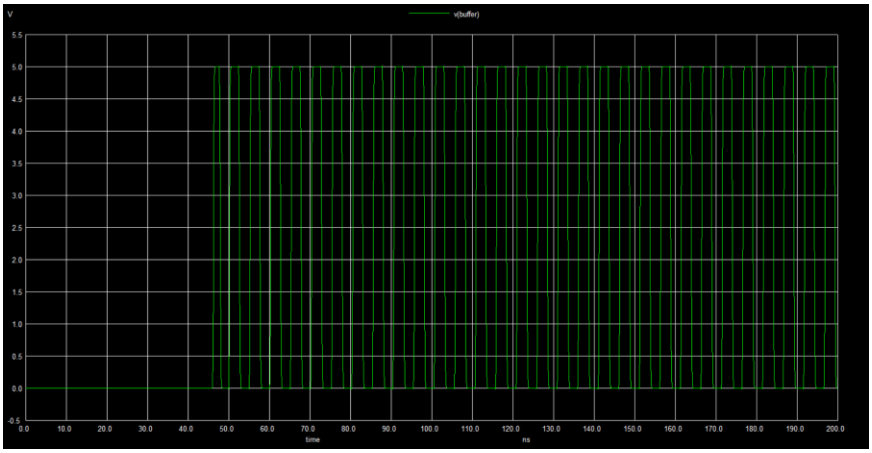

Fig. 9: Buffer output when V_{in}=1.2V

The buffered output waveform shows clean square wave transitions compared to the VCO output. For VIN = 0.7V, the frequency is lower, while for VIN = 1.2V, the frequency increases, consistent with the behavior of the VCO. The use of four cascaded inverters improves the signal quality by sharpening the rise and fall times, converting the non-ideal oscillator output into a stable digital waveform suitable for further processing.

COUNTER OUTPUT (Q0–Q3)

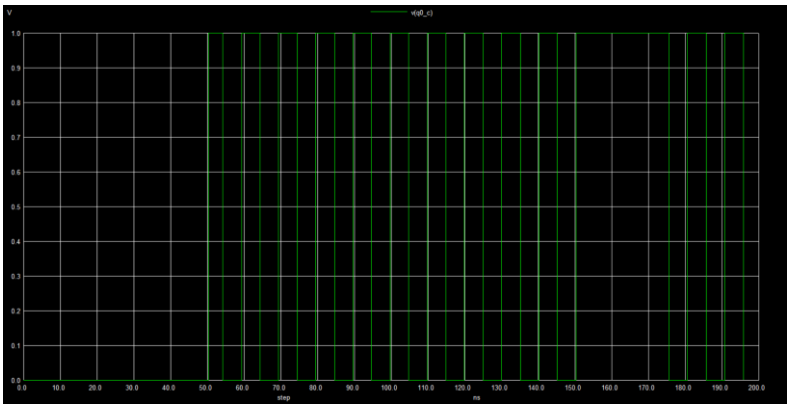

Fig. 10: Counter Output Q0 for VIN = 1.2V

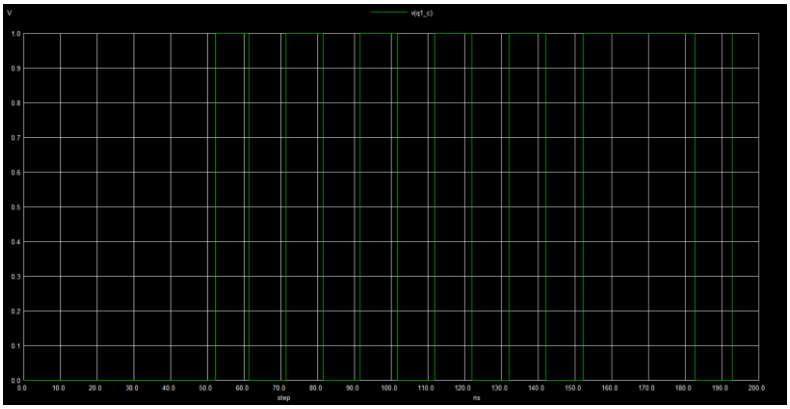

Fig. 10: Counter Output Q1 for VIN = 1.2V

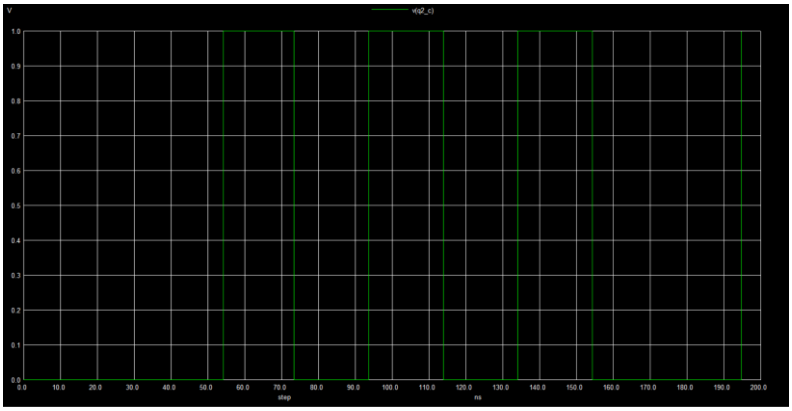

Fig. 10: Counter Output Q2 for VIN = 1.2V

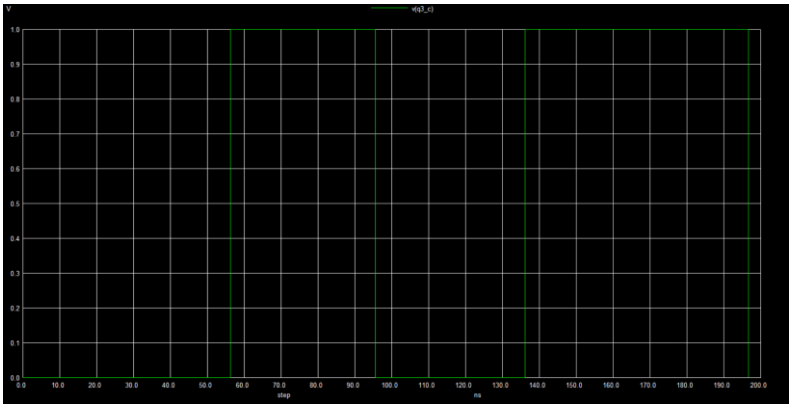

Fig. 10: Counter Output Q3 for VIN = 1.2V

The counter outputs (Q0–Q3) show the binary counting sequence corresponding to the pulses received during the sampling window for VIN = 1.2V. The outputs toggle in a ripple manner, confirming correct operation of the 4-bit asynchronous counter.

For VIN = 1.2V, the oscillation frequency is moderate, resulting in a corresponding count value within the 4-bit range. This demonstrates that the counter output accurately reflects the input voltage through the frequency of the VCO.

LATCH OUTPUTS

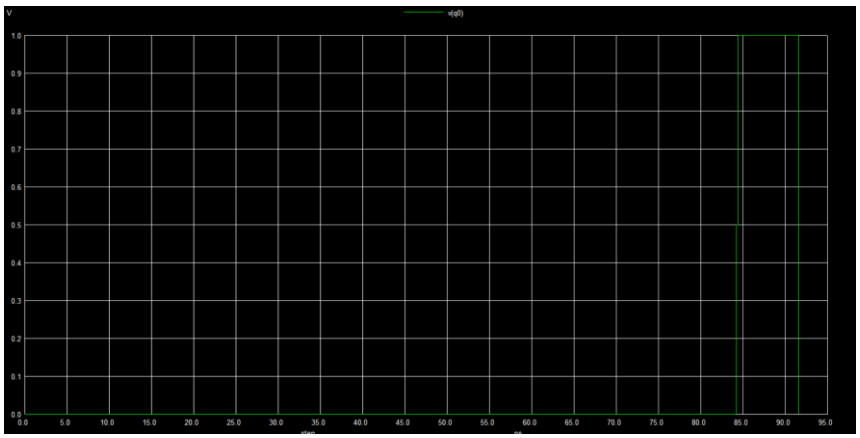

Fig. 17: Latched Output Q0 for VIN = 1.2V

The Q0 waveform exhibits a logic high transition within the sampling interval of approximately 80–90 ns. Although the transition does not occur exactly at 81 ns due to propagation delays, the presence of a high level within this window confirms a valid logic ‘1’. Hence, Q0 is considered as 1.

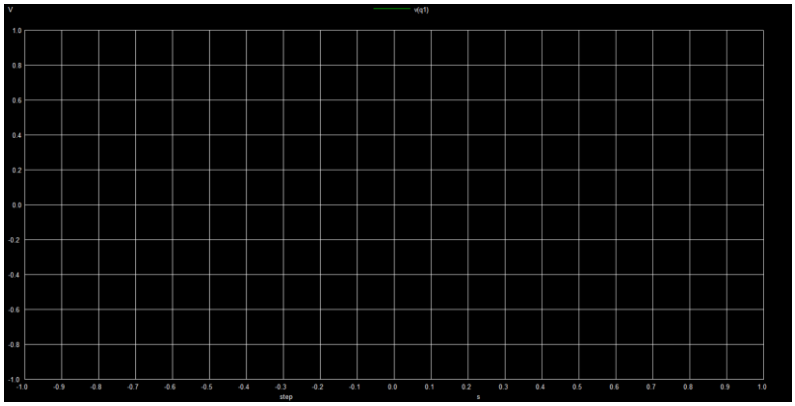

Fig. 16: Latched Output Q1 for VIN = 1.2V

The Q1 waveform remains at logic low throughout the sampling interval (80–90 ns) and does not exhibit any high level. Therefore, Q1 is interpreted as logic ‘0’.

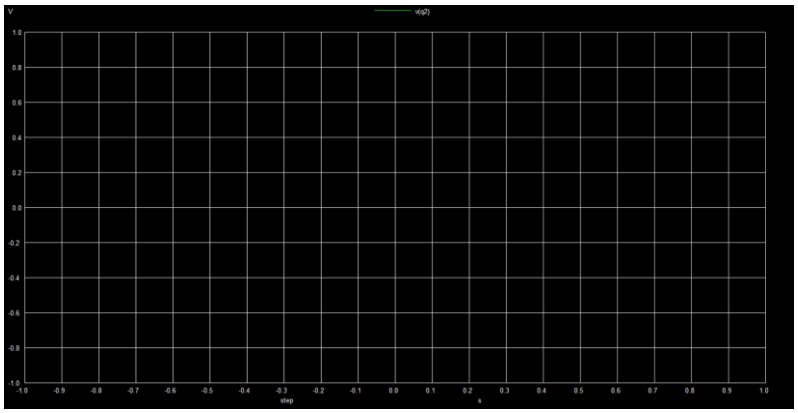

Fig. 16: Latched Output Q2 for VIN = 1.2V

The Q2 waveform also remains at logic low within the sampling window and does not show any high signal. Hence, Q2 is considered as logic ‘0’.

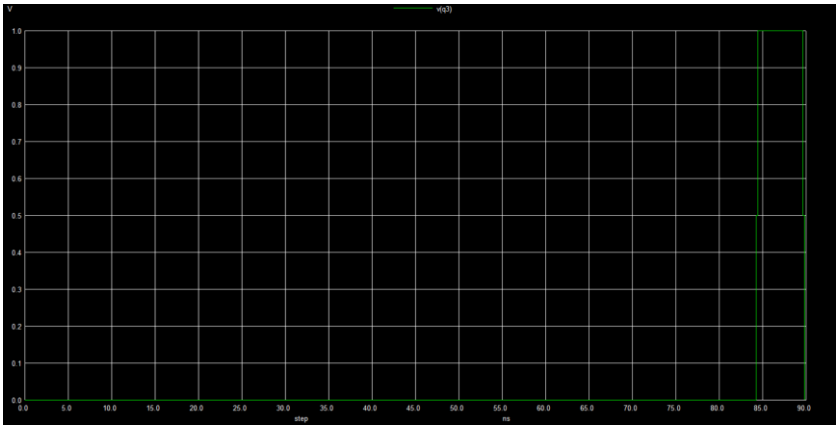

Fig. 14: Latched Output Q3 for VIN = 1.2V

The Q3 waveform shows a logic high level within the 80–90 ns interval. Even though exact alignment with 81 ns may vary due to propagation delays, the presence of a high signal within this window confirms a logic ‘1’. Thus, Q3 is taken as 1.

Interpretation Criterion:
The digital output is determined by observing the logic level of each counter output within the defined sampling window (80–90 ns). If a signal attains a logic high level within this interval, it is interpreted as '1'; otherwise, if the signal remains low throughout the interval, it is interpreted as '0'. This approach accounts for propagation delays and ensures reliable data capture.

The outputs are interpreted in the order Q3 Q2 Q1 Q0: 1001

Practical Observations:
The effective operating range of the input voltage begins from approximately 0.7 V, which corresponds to the threshold voltage of the MOS transistors. Below this voltage, the VCO does not generate sufficient oscillations, and hence the ADC does not produce a valid output. The following outputs are observed from simulation:

VIN (V)	Output (Q3 Q2 Q1 Q0)
0.7	0000
1.2	1001
2.5	1100
3.0	1110

It is observed that as the input voltage increases, the digital output also increases, confirming the expected behavior of the ADC.

DISCUSSIONS

The simulation results demonstrate that the proposed VCO-based ADC operates correctly based on the principle of time-domain conversion. As the input voltage increases, the oscillation frequency of the VCO increases, resulting in a higher number of pulses counted within the sampling window. This leads to a corresponding increase in the digital output, confirming correct ADC behavior.

The relationship between the input voltage and the counter output can be expressed as:

$$N = f_{out} \cdot T_s$$

where N is the counter output, f_{out} is the VCO frequency, and T_s is the sampling time.

Since the VCO frequency is proportional to the input voltage,

$$f_{out} = K_{VCO} \cdot V_{IN}$$

Combining both,

$$N = K_{VCO} \cdot V_{IN} \cdot T_s$$

CONCLUSION

The VCO-based Analog-to-Digital Converter was successfully designed and implemented using a time-domain conversion approach. The system effectively converts the input analog voltage into a corresponding digital output through voltage-to-frequency conversion and pulse counting.

The design was verified using simulation in the eSim platform, and the results obtained at different stages confirm correct operation of each block. The observed outputs match the expected behavior, with higher input voltages producing higher digital counts.

Thus, the proposed system successfully demonstrates the working principle of a VCO-based ADC and achieves the desired functionality.

REFERENCES

[1] J. Kim, S. Lee, and K. Lee, "A Time-to-Digital Converter-Based Analog-to-Digital Converter," IEEE Journal of Solid-State Circuits, 2010.

[2] J. Kim, T.-K. Jang, Y.-G. Yoon, and S. Cho, "Analysis and Design of Voltage-Controlled Oscillator Based Analog-to-Digital Converter," IEEE Transactions on Circuits and Systems, 2009.

[3] P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, 2nd ed. New York, NY, USA: Oxford University Press, 2002.

[4] M. J. M. Pelgrom, Analog-to-Digital Conversion. Dordrecht, Netherlands: Springer, 2010.

[5] Analog Devices, "Time-Based ADC Overview," Application Note, 2015.

[6] Texas Instruments, "ADC Basics," Application Report, 2014.