ABSTRACT

Title of the Research Migration Project:

DESIGN AND SIMULATION OF A CMOS SCHMITT TRIGGER USING ESIM FOR HYSTERESIS-BASED SIGNAL CONDITIONING

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Theory / Description

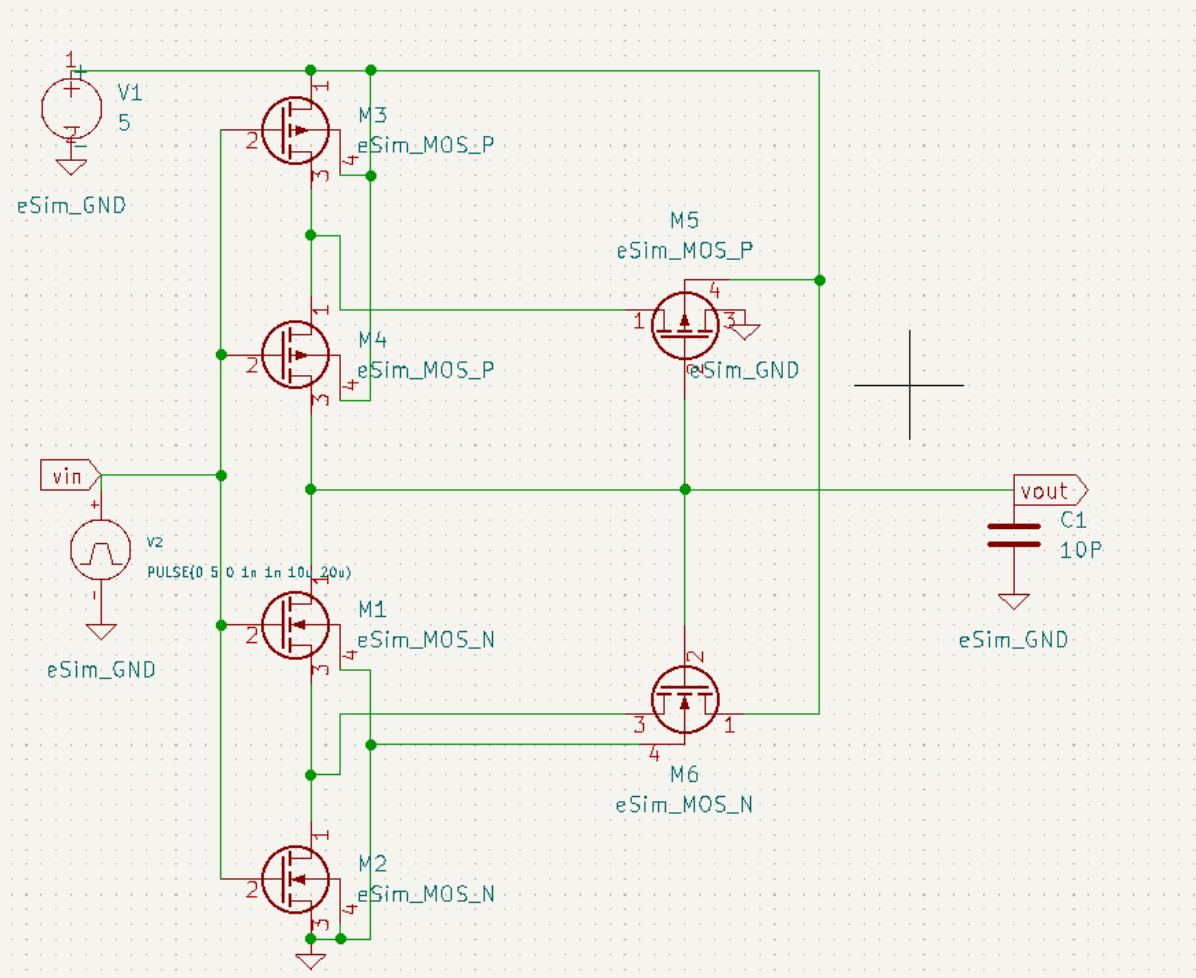
A Schmitt Trigger is a regenerative comparator circuit that incorporates **positive feedback** to introduce hysteresis. Unlike a conventional inverter, which switches at a single threshold voltage, a Schmitt Trigger has **two distinct switching thresholds**: an upper threshold (VTH+) and a lower threshold (VTH−). This property makes it highly effective in eliminating noise from input signals.

In this project, a CMOS Schmitt Trigger is designed using complementary MOS transistors (PMOS and NMOS). The circuit consists of a pull-up network (PMOS), a pull-down network (NMOS), and additional feedback transistors that reinforce switching behavior.

When the input voltage increases, the feedback mechanism delays switching until the input crosses a higher threshold voltage (VTH+). Similarly, when the input decreases, the output switches back at a lower threshold (VTH−). This difference between the two thresholds forms the **hysteresis loop**, which ensures stable output even in the presence of noise or slow input transitions.

The circuit is simulated using eSim (Ngspice backend), and its behavior is analyzed using transient analysis.

Circuit Diagram:



Explanation:

- PMOS transistors are connected to VDD (5V) forming the pull-up network
- NMOS transistors are connected to ground forming the pull-down network
- Feedback transistors introduce hysteresis
- Input (Vin) is applied using a pulse source
- Output (Vout) is taken across the load capacitor

Results / Output

The circuit is simulated using transient analysis with a pulse input signal varying between 0V and 5V.

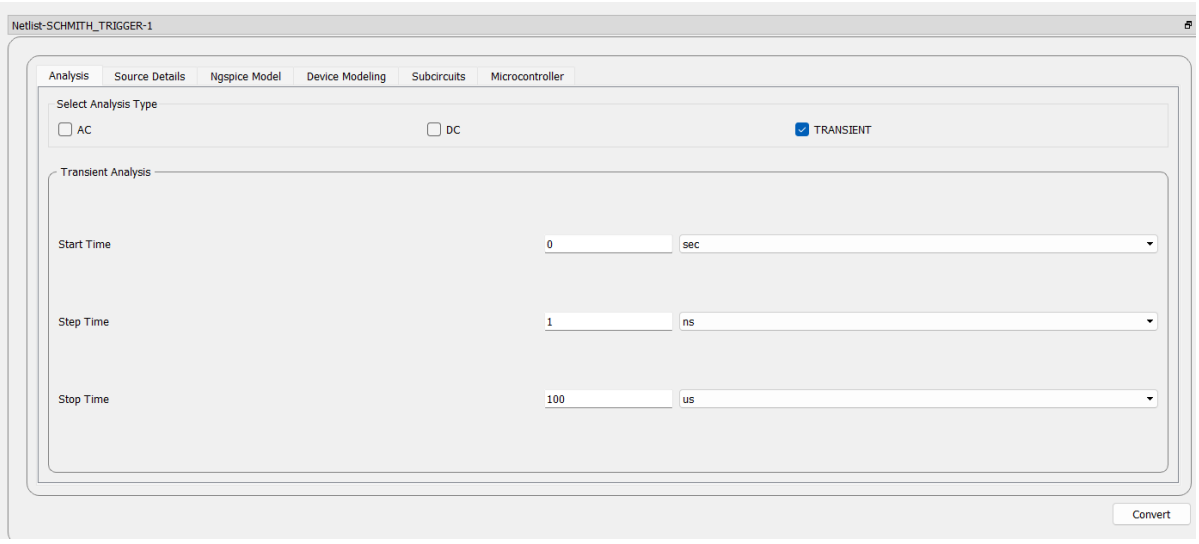
Observations:

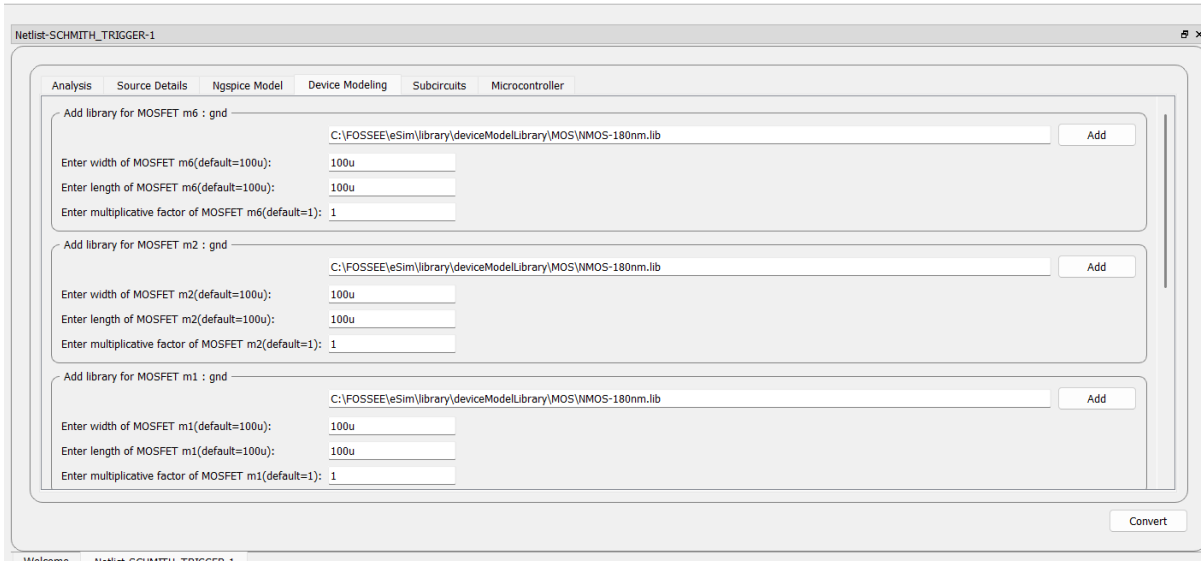
- The input signal (Vin) is a square wave
- The output signal (Vout) switches between 0V and 5V
- The switching of output does not occur at the same input voltage for rising and falling edges
- This confirms the presence of **hysteresis**

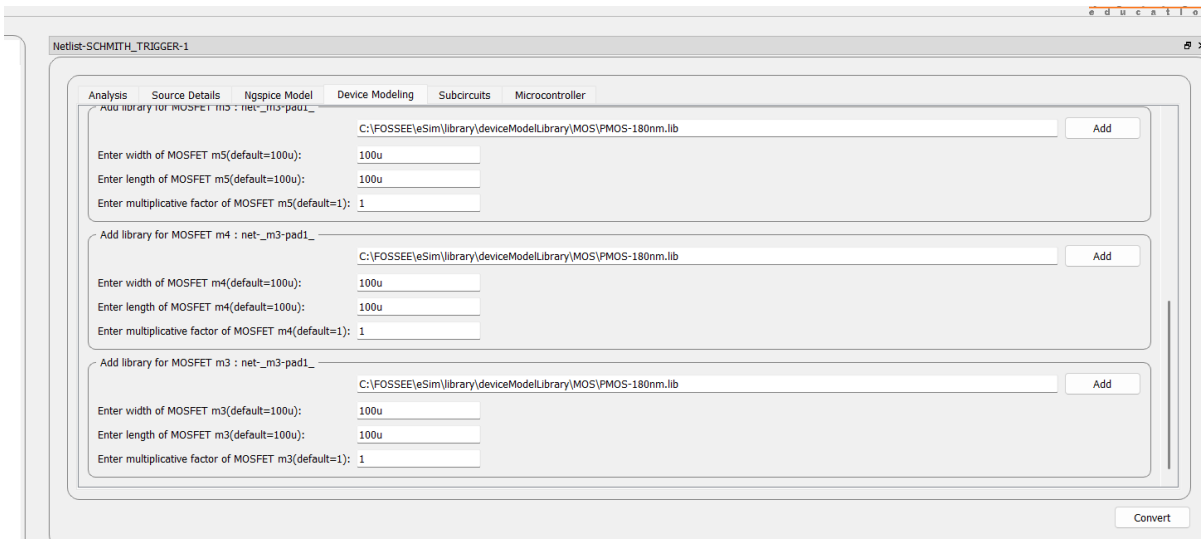
The output waveform shows:

- Smooth rising edges due to capacitive charging
- Faster falling edges due to NMOS discharge path

This behavior validates that the designed circuit functions as a **Schmitt Trigger**, providing noise immunity and stable switching.




Netlist-SCHMITH_TRIGGER-1
Analysis
Source Details
Ngspice Model
Device Modeling
Subcircuits
Microcontroller
Add library for MOSFET m6 : gnd
C:\FOSSEE\eSim\library\deviceModelLibrary\MOS\NMOS-180nm.lib
Add
Enter width of MOSFET m6(default=100u):
100u
Enter length of MOSFET m6(default=100u):
100u
Enter multiplicative factor of MOSFET m6(default=1):
1
Add library for MOSFET m2 : gnd
C:\FOSSEE\eSim\library\deviceModelLibrary\MOS\NMOS-180nm.lib
Add
Enter width of MOSFET m2(default=100u):
100u
Enter length of MOSFET m2(default=100u):
100u
Enter multiplicative factor of MOSFET m2(default=1):
1
Add library for MOSFET m1 : gnd
C:\FOSSEE\eSim\library\deviceModelLibrary\MOS\NMOS-180nm.lib
Add
Enter width of MOSFET m1(default=100u):
100u
Enter length of MOSFET m1(default=100u):
100u
Enter multiplicative factor of MOSFET m1(default=1):
1
Convert


Netlist-SCHMITH_TRIGGER-1
Analysis
Source Details
Ngspice Model
Device Modeling
Subcircuits
Microcontroller
C:\FOSSEE\eSim\library\deviceModelLibrary\MOS\PMOS-180nm.lib
Add
Enter width of MOSFET m5(default=100u):
100u
Enter length of MOSFET m5(default=100u):
100u
Enter multiplicative factor of MOSFET m5(default=1):
1
Add library for MOSFET m4 : net-_m3-pad1_
C:\FOSSEE\eSim\library\deviceModelLibrary\MOS\PMOS-180nm.lib
Add
Enter width of MOSFET m4(default=100u):
100u
Enter length of MOSFET m4(default=100u):
100u
Enter multiplicative factor of MOSFET m4(default=1):
1
Add library for MOSFET m3 : net-_m3-pad1_
C:\FOSSEE\eSim\library\deviceModelLibrary\MOS\PMOS-180nm.lib
Add
Enter width of MOSFET m3(default=100u):
100u
Enter length of MOSFET m3(default=100u):
100u
Enter multiplicative factor of MOSFET m3(default=1):
1
Convert

```
Initial Transient Solution
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Node                                   Voltage
----                                   -------
net-_m3-pad1_                                5
vout                                         5
net-_m1-pad3_                          4.14721
vin                                          0
net-_m3-pad3_                                5
v1#branch                       -4.00066e-11
v2#branch                                    0
```
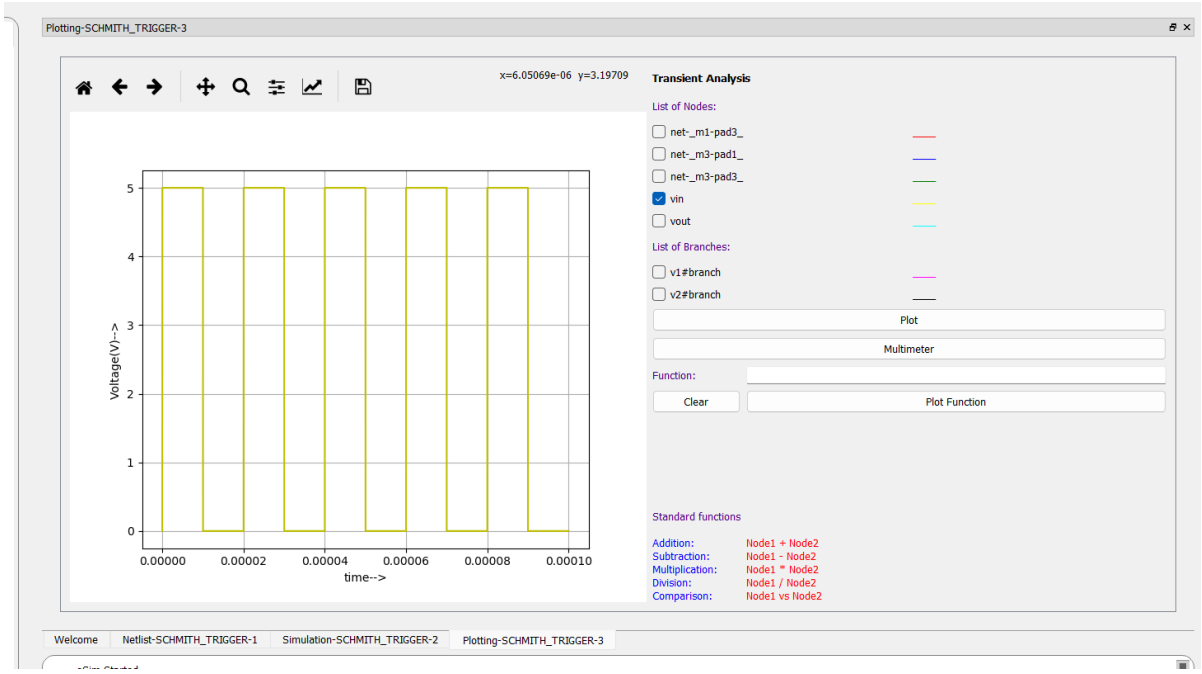
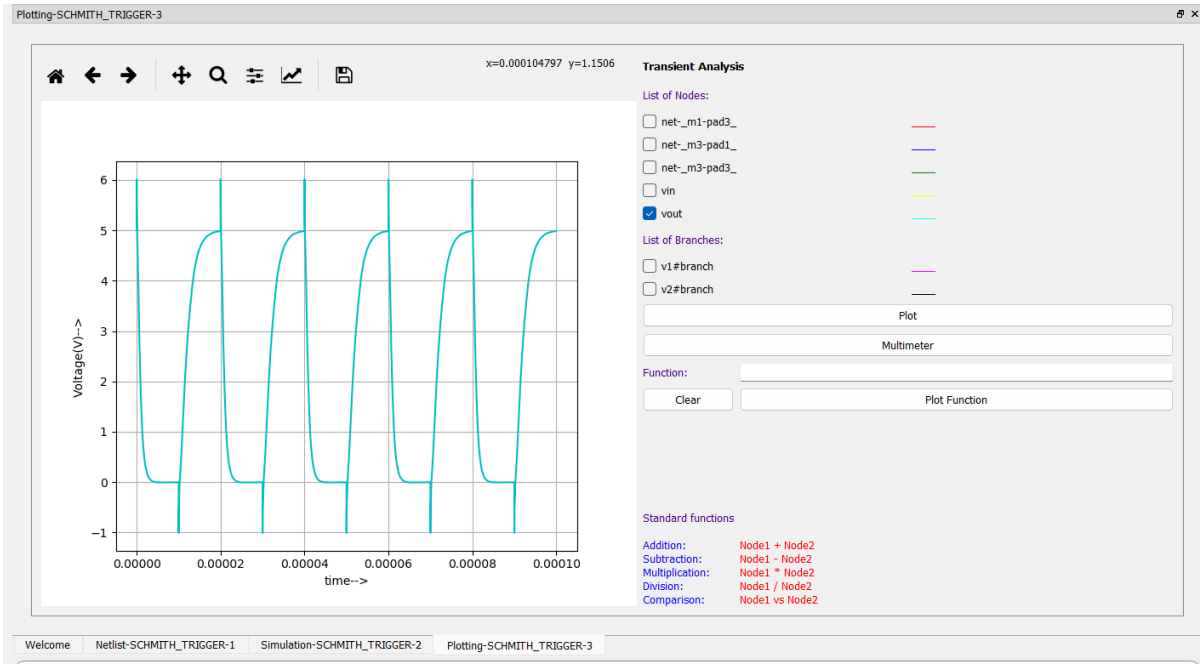
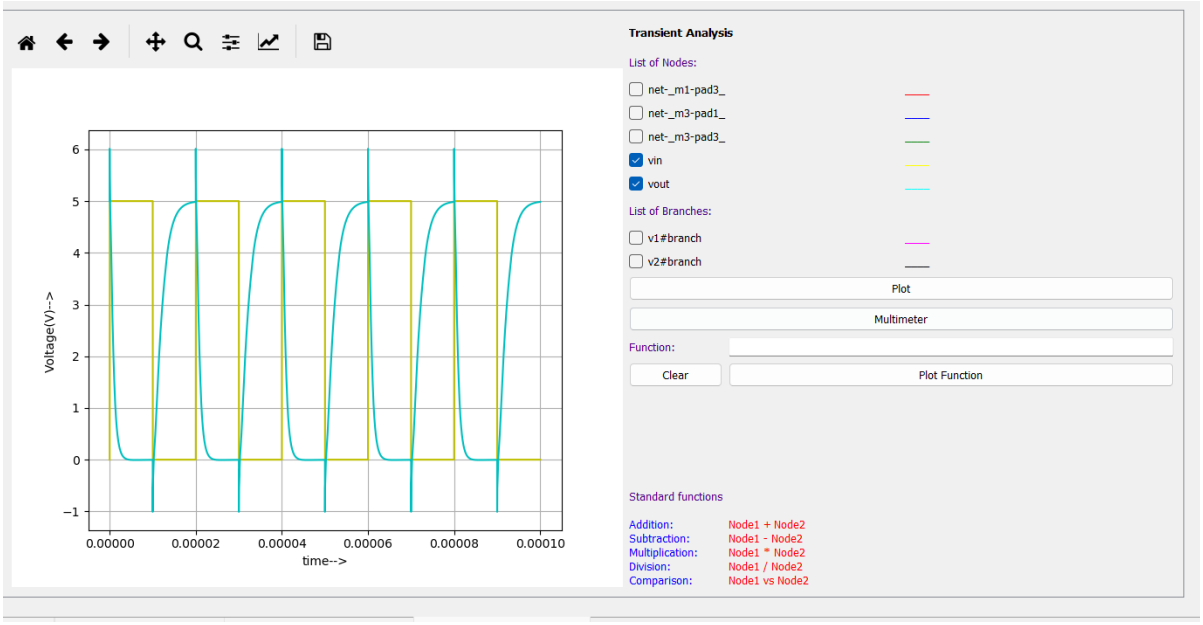
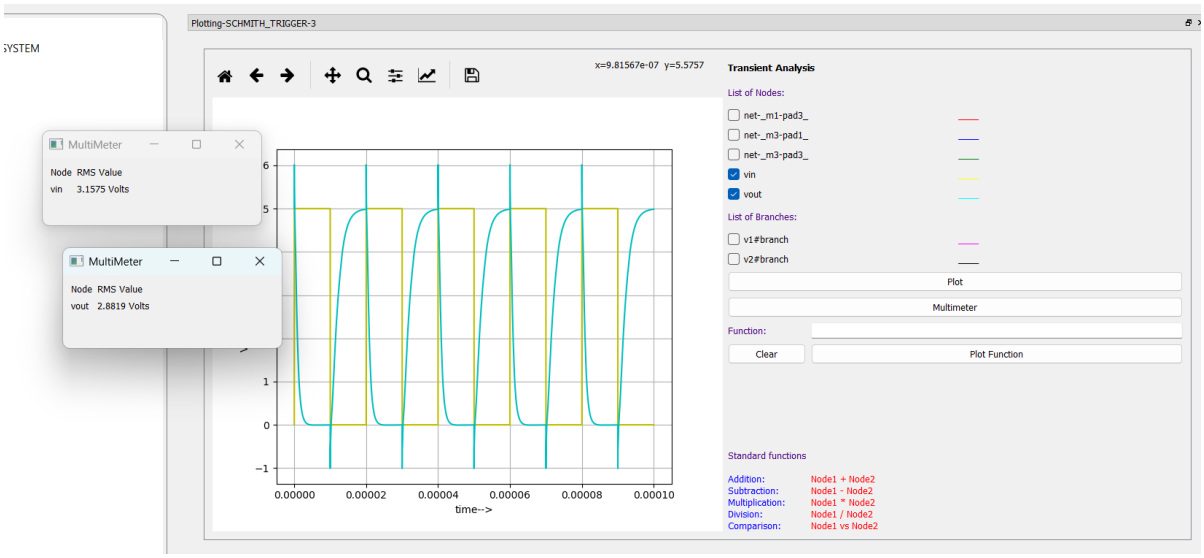




Plotting-SCHMITH_TRIGGER-3
x=0.000104797 y=1.1506
Voltage(V)-->
time-->
Transient Analysis
List of Nodes:
net-_m1-pad3_
net-_m3-pad1_
net-_m3-pad3_
vin
vout
List of Branches:
v1#branch
v2#branch
Plot
Multimeter
Function:
Clear
Plot Function
Standard functions
Addition: Node1 + Node2
Subtraction: Node1 - Node2
Multiplication: Node1 * Node2
Division: Node1 / Node2
Comparison: Node1 vs Node2
Welcome
Netlist-SCHMITH_TRIGGER-1
Simulation-SCHMITH_TRIGGER-2
Plotting-SCHMITH_TRIGGER-3


Voltage(V)-->
time-->
Transient Analysis
List of Nodes:
net-_m1-pad3_
net-_m3-pad1_
net-_m3-pad3_
vin
vout
List of Branches:
v1#branch
v2#branch
Plot
Multimeter
Function:
Clear
Plot Function
Standard functions
Addition: Node1 + Node2
Subtraction: Node1 - Node2
Multiplication: Node1 * Node2
Division: Node1 / Node2
Comparison: Node1 vs Node2



The CMOS Schmitt trigger converts a slowly varying input into a digital output. The output switches between two levels and exhibits hysteresis, meaning the switching thresholds for rising and falling inputs are different.

References

1. FOSSEE eSim Documentation
2. Sedra, A. S., & Smith, K. C., *Microelectronic Circuits*
3. Weste, N. H. E., & Harris, D., *CMOS VLSI Design*
4. Ngspice User Manual
5. Analysis and Design of the Classical CMOS Schmitt Trigger in Subthreshold Operation Author: L. A. P. Melek et al.