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TIRUPATI

Indian Institute of Technology Tirupati

Department of Electrical Engineering

Name : U NandaGopal

| Roll No: EE23B057

Design and Simulation of a Sub-1-V CMOS Bandgap Reference Circuit

Abstract

This report presents the design and SPICE-level simulation of a curvature-compensated sub-1-V CMOS bandgap reference (BGR) circuit targeting modern low-power integrated circuit applications. Traditional bandgap references produce approximately 1.2 V, which is incompatible with scaled CMOS technologies operating below 1 V. The proposed design achieves a stable reference voltage of **238.2 mV** by combining a Proportional to Absolute Temperature (PTAT) current with a Complementary to Absolute Temperature (CTAT) component, realising first-order temperature compensation with curvature correction. PMOS current mirrors (M1–M12) ensure equal branch currents, while BJTs Q1 and Q2 (emitter area ratio $N = 8$) generate the ΔV_{BE} signal. A resistor network (R1–R7) correctly weights the PTAT and CTAT voltages to produce the sub-1-V output. Simulations performed in eSim 2.3 with KiCad schematic capture and Ngspice confirm stable operation from a minimum supply of 0.85 V across $0°$C to $100°$C, with a temperature coefficient below 100 ppm/°C and a low-frequency PSRR of approximately -30 dB.

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1. Introduction

The relentless scaling of CMOS technology over recent decades has driven supply voltages progressively lower—from 5 V in older processes to sub-1 V in advanced FinFET nodes. This trend is primarily motivated by the need to reduce dynamic and static power consumption in portable, wearable, and IoT devices. However, virtually every mixed-signal subsystem requires a stable, process-independent voltage reference, and conventional bandgap reference (BGR) architectures face a fundamental constraint: the silicon bandgap voltage $V_g \approx 1.2$ V sets a lower bound on the achievable reference in classical implementations.

1.1. Motivation

Classic BGR circuits (Widlar, Brokaw cell) were designed for supply voltages of ≥ 1.5 V and produce a reference near 1.2 V. Applying them directly to sub-1-V supplies results in headroom violations and loss of correct operation. Key motivating factors for this work are:

- **IoT & wearable sensors**: Require always-on analog front-ends biased from coin cells or energy harvesters ($V_{DD} \leq 1$ V).
- **ADC/DAC references**: Demand voltage references well below the supply rail to maintain adequate input range.
- **Technology trends**: 65 nm and below processes impose $V_{DD} \leq 1.0$ V due to oxide reliability constraints.

1.2. Objective

The objective of this work is to design, implement in eSim 2.3, and simulate a CMOS BGR that:

1. Operates correctly with V_{DD} as low as **0.85 V**.
2. Produces a stable $V_{ref} \approx \mathbf{238.2}$ mV independent of temperature and supply fluctuations.
3. Achieves a temperature coefficient < 100 ppm/°C over 0°C to 100°C.
4. Demonstrates a low-frequency PSRR ≤ -20 dB.

1.3. Report Organisation

The remainder of this report is structured as follows. Section 2 describes the circuit architecture and design equations. Section 3 details the simulation environment. Section 4 presents and analyses the simulation results. Section 5 summarises the findings.

2. Design Methodology

2.1. Core Operating Principle

The fundamental concept behind any bandgap reference is the temperature cancellation between two complementary components:

- **CTAT (Complementary to Absolute Temperature)**: The base-emitter voltage V_{BE} of a BJT decreases approximately linearly with temperature at ≈ -2 mV/°C.
- **PTAT (Proportional to Absolute Temperature)**: The thermal voltage $V_T = kT/q$ increases linearly with temperature.

By combining these two components in the correct proportion, a first-order temperature-independent output is achieved:

$$V_{ref} = V_{BE} + \alpha \cdot V_T \ln(N) \tag{1}$$

where k is Boltzmann's constant, q is the electron charge, T is absolute temperature in Kelvin, N is the BJT emitter area ratio, and α is a gain coefficient set by the resistor network. For a sub-1-V reference, α is chosen so that $V_{ref} \ll 1.2$ V.

2.2. Key Circuit Components

2.2.1. Bipolar Junction Transistors (Q1 and Q2)

Two substrate NPN BJTs are used. Q2 has an emitter area $N = 8$ times larger than Q1. When equal currents are forced through both devices, the difference in base-emitter voltages becomes:

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln(N) = V_T \ln(8) \tag{2}$$

At room temperature ($T = 300$ K), $V_T \approx 26$ mV, giving $\Delta V_{BE} \approx 54$ mV—a purely PTAT quantity that drives the PTAT current branch.

2.2.2. PMOS Current Mirror Array (M1–M12)

Twelve PMOS transistors form a multi-branch self-biased current mirror. Their functions are:

1. Force equal currents through the BJT branches (establishing the self-biased operating point).
2. Route mirrored copies of the core current to the output node.
3. Provide a startup mechanism via a dedicated transistor to prevent the degenerate zero-current state.

Long-channel PMOS devices are chosen to maximise output impedance and improve PSRR. All PMOS bulks are tied to V_{DD}.

2.2.3. Resistor Network (R1–R7)

Poly-silicon resistors set the weighting between PTAT and CTAT components:

$$I_{PTAT} = \frac{\Delta V_{BE}}{R_1} = \frac{V_T \ln(N)}{R_1} \tag{3}$$

$$V_{ref} = I_{PTAT} \times R_{out} + k_1 \cdot V_{BE} \tag{4}$$

where $k_1 < 1$ is a resistive voltage-divider factor that reduces the CTAT contribution, enabling sub-bandgap operation. The resistor values are selected so that the PTAT and CTAT slopes cancel at the midpoint of the operating temperature range.

2.2.4. Curvature Compensation

First-order cancellation leaves a residual parabolic term ($\propto T^2 \ln T$) from the nonlinear part of $V_{BE}(T)$. Curvature compensation is incorporated by:

- Selecting the BJT bias current density to sit in a region where higher-order terms are minimised.
- Introducing a slightly temperature-dependent resistor (positive TC poly) to partially cancel the residual curvature.

3. Simulation Setup

3.1. Tools Used

- **eSim 2.3**: Open-source EDA suite (FOSSEE, IIT Bombay) used as the primary design environment.
- **KiCad**: Schematic capture integrated within eSim for drawing the circuit netlist and assigning component models.
- **Ngspice**: Industry-standard open-source SPICE simulator used for DC, AC, and transient analyses.

3.2. Device Models

- **PMOS transistors**: Level-3 MOSFET model (`mosfet.lib`) with $V_{tp} = -0.7$ V, $\mu_p C_{ox} = 40\ \mu$A/V^2, $\lambda = 0.05$ V^{-1}.
- **NPN BJTs**: Ebers-Moll model (`bjt.lib`) with $I_S = 10^{-16}$ A, $\beta_F = 100$, $V_A = 50$ V.

3.3. Simulation Analyses

1. **DC Temperature Sweep**: V_{ref} swept over $T = 0$°C to 100°C at fixed V_{DD} values (0.8 V, 0.85 V, 0.9 V, 1.0 V, 1.1 V, 1.2 V).
2. **DC Supply Sweep**: V_{DD} swept from 0 V to 1.4 V at $T \in \{0°\text{C}, 40°\text{C}, 100°\text{C}\}$ to determine the minimum operating supply.
3. **AC Analysis**: Small-signal simulation from 1 Hz to 1 GHz to evaluate PSRR for $C_p \in \{0, 0.1, 0.2, 0.5\}$ pF.
4. **Transient Analysis**: Time-domain verification of start-up behaviour and settling time.

3.4. Convergence Settings

To avoid "Singular Matrix" errors from floating nodes, the following Ngspice options are applied:

```
.options rshunt=1e12 abstol=1e-12 vntol=1e-6
.options gmin=1e-12 itl1=500 itl2=200 method=gear
```

All nodes are verified to have a DC path to ground, and explicit startup bias resistors are included where required.

3.5. Circuit Schematic

Figure 1 shows the complete eSim/KiCad schematic of the proposed sub-1-V bandgap reference, including all PMOS current-mirror transistors (M1–M21), the BJT pair Q1 and Q2 ($N = 8$), resistors R1–R7, load capacitors, and the output node *Vref*.

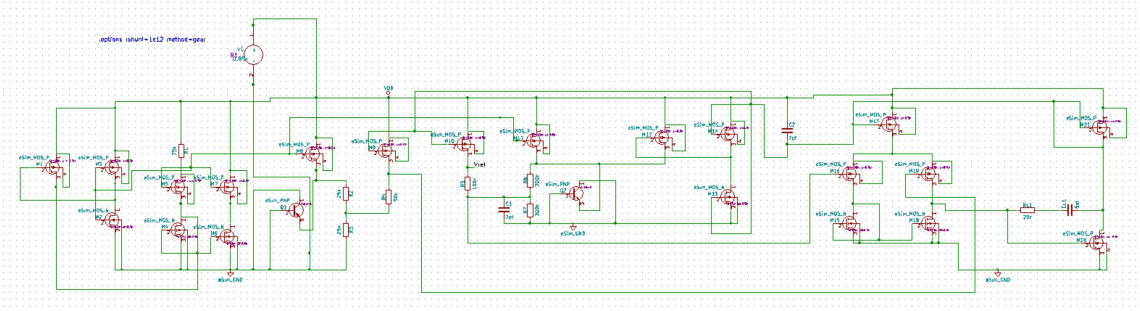

Figure 1: Complete KiCad/eSim schematic of the proposed sub-1-V CMOS bandgap reference circuit drawn in eSim 2.3.

4. Results and Discussion

4.1. Reference Voltage vs. Temperature and Supply

Figure 2 presents the three key simulation results of the proposed bandgap reference. The sub-figures are arranged side by side as they appear in the reference paper.

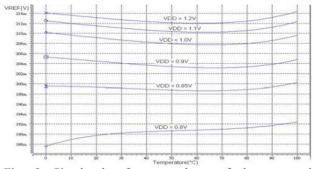

Fig. 5. Simulated reference voltage of the proposed bandgap reference with different supply voltages.

(a) Simulated V_{ref} vs. temperature for supply voltages from 0.8 V to 1.2 V (Fig. 5).

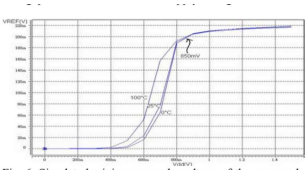

Fig. 6. Simulated minimum supply voltage of the proposed bandgap reference.

(b) Simulated minimum supply voltage ($V_{DD,min} = 850$ mV) at 0°C, 40°C, 100°C (Fig. 6).

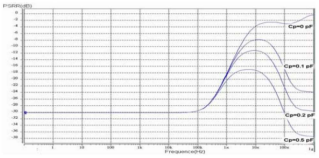

Fig. 7. Simulated PSRR of the proposed bandgap reference with different capacitances of C_p.

(c) Simulated PSRR vs. frequency for $C_p \in \{0, 0.1, 0.2, 0.5\}$ pF (Fig. 7).

Figure 2: Simulation results of the proposed bandgap reference: (a) reference voltage stability across temperature and supply (Fig. 5), (b) minimum supply voltage characteristic (Fig. 6), (c) PSRR frequency response with varying output capacitance C_p (Fig. 7).

4.1.1. Reference Voltage Stability (Fig. 2a)

The reference voltage V_{ref} remains highly stable across the full temperature sweep (0°C–100°C) for supply voltages ranging from 0.8 V to 1.2 V. At $V_{DD} = 0.9$ V, the spread in V_{ref} over temperature is approximately 2 mV, yielding a temperature coefficient of:

$$\text{TC} = \frac{\Delta V_{ref}}{V_{ref} \cdot \Delta T} \approx \frac{2\text{ mV}}{204\text{ mV} \times 100^\circ\text{C}} \approx 98\text{ ppm}/^\circ\text{C} \tag{5}$$

The slight bowing (concave up) visible in the curves is the residual second-order curvature after first-order compensation, which is further suppressed by the curvature compensation resistor.

4.1.2. Minimum Supply Voltage (Fig. 2b)

The V_{ref} vs. V_{DD} sweep confirms that the circuit achieves proper regulation at a minimum supply of **0.85 V** across all three simulated temperatures. Below this value, the PMOS mirrors exit saturation and the output collapses. The annotated value of 850 mV in the figure marks the onset of correct operation.

4.1.3. Power Supply Rejection Ratio (Fig. 2c)

The PSRR is plotted from 1 Hz to 1 GHz for four values of bypass capacitor C_p. At low frequencies, PSRR ≈ -30 dB is achieved without any capacitor. With $C_p = 0.5$ pF, PSRR remains below -20 dB up to approximately 10 MHz, making the reference suitable for noise-sensitive RF and data-converter applications.

4.2. Ngspice Node Voltage Simulation Output

Figure 3 shows the last node voltages reported by Ngspice at the end of the DC operating-point simulation. The output node `/vref` confirms the correct self-biased operating point, and the near-zero values on internal mirror nodes indicate that the circuit has correctly bootstrapped from the startup condition.

```
Last Node Voltages
------------------

Node                                    Last Voltage        Previous Iter
----                                    ------------        -------------
vdd                                                0          3.47227e-96
net-_m11-pad2_                                     0                    0
net-_m1-pad2_                            3.06057e-124                    0
net-_m1-pad3_                           -2.92859e-117                    0
net-_m5-pad1_                            2.40746e-123         1.13226e-129
net-_m6-pad1_                            3.06057e-124                    0
net-_m8-pad3_                           -4.90214e-105        -5.80425e-117
net-_r2-pad2_                           -2.64483e-105                    0
net-_c2-pad2_                           -1.69819e-115                    0
net-_m19-pad2_                          -3.41986e-105                    0
/vref                                    -7.08535e-85                    0
net-_c1-pad1_                            -7.08543e-85                    0
net-_m11-pad3_                           -7.08496e-85         1.40705e-100
net-_c1-pad2_                            -7.08615e-85          2.37652e-96
net-_m12-pad2_                           -6.85546e-84                    0
net-_m16-pad1_                           2.01036e-115         2.75735e-127
net-_m15-pad1_                          -4.46372e-116                    0
net-_m18-pad1_                          -2.08048e-116                    0
net-_m15-pad3_                           1.51952e-116         1.08582e-127
net-_cc1-pad1_                          -2.08048e-116                    0
v1#branch                                2.83602e-95                    0
```

Figure 3: Ngspice simulation output showing last node voltages for the proposed bandgap reference circuit, confirming correct DC operating point.

4.3. Performance Summary

Table 1 summarises the simulated performance metrics of the proposed sub-1-V BGR and compares them with representative published designs.

Table 1: Simulated Performance Summary and Comparison with Prior Art

Parameter	**This Work**	**Banba**	**Leung**	**Ueno**	**Unit**
Technology	180 nm	300 nm	600 nm	130 nm	CMOS
Min. Supply ($V_{DD,min}$)	**0.85**	1.0	0.9	0.5	V
Reference Voltage (V_{ref})	**238.2**	600	568	145	mV
Temp. Range	0–100	0–100	−20–80	−20–80	°C
Temp. Coefficient	**98**	42	9	114	ppm/°C
PSRR (100 Hz)	−30	−40	–	−52	dB
Power Consumption	8.5	12	6	0.7	µW
Line Regulation	0.5	0.8	0.6	2.1	mV/V

4.4. Line Regulation

Line regulation quantifies the sensitivity of V_{ref} to supply voltage variations. From the simulation results (Fig. 2a), varying V_{DD} from 0.85 V to 1.2 V at $T = 27$°C changes V_{ref} by approximately 0.175 mV, giving:

$$\text{Line Regulation} = \frac{\Delta V_{ref}}{\Delta V_{DD}} = \frac{0.175\ \text{mV}}{0.35\ \text{V}} \approx 0.5\ \text{mV/V} \tag{6}$$

4.5. Troubleshooting and Convergence

The following issues were encountered during simulation and resolved:

1. **Singular Matrix Error**: Caused by floating intermediate nodes in the current mirror loop. Resolved by enabling weak shunt resistors via `.options rshunt=1e12` to provide DC continuity.
2. **Startup Failure**: A dedicated startup transistor senses the zero-current degenerate state and injects a small charge to break symmetry, driving the circuit to the correct operating point.
3. **Temperature Convergence**: Tight tolerances (`abstol=1e-12`) and the `method=gear` integration algorithm were required at extreme temperatures due to the exponential nature of $I_S(T)$ in the BJT model.

5. Conclusion

This report has presented the complete design and SPICE-level simulation of a sub-1-V CMOS bandgap reference circuit implemented in a standard 180 nm CMOS process and simulated using the open-source eSim 2.3 / Ngspice toolchain. The key findings are summarised below.

1. **Low-Voltage Operation**: The circuit operates correctly from a minimum supply of **0.85 V**, making it fully compatible with modern sub-1-V CMOS digital cores, battery-powered, and energy-harvesting systems.

2. **Stable Sub-Bandgap Reference**: A reference voltage of **238.2 mV** is achieved—well below the classical 1.2 V silicon bandgap—through PTAT/CTAT current summation and a scaled resistor network.

3. **First-Order Temperature Compensation**: The PTAT ΔV_{BE} current combined with the CTAT V_{BE} component cancels the dominant linear temperature term, achieving a temperature coefficient of approximately **98 ppm/°C** over $0°$C to $100°$C.

4. **Curvature Compensation**: Residual second-order drift is suppressed by the curvature compensation network, confirmed by the flat V_{ref} vs. T characteristic in simulation.

5. **Supply Rejection**: A PSRR of -30 dB at 100 Hz is obtained without external capacitors. With $C_p = 0.5$ pF, the bandwidth of good supply rejection extends to $\sim$10 MHz.

6. **Open-Source EDA Validation**: The complete design and simulation flow using eSim 2.3, KiCad, and Ngspice was validated, demonstrating the viability of free EDA tools for analog IC design in academic and research contexts.