Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit : Implement 32-bit RISC-V Architecture Processor using Verilog HDL

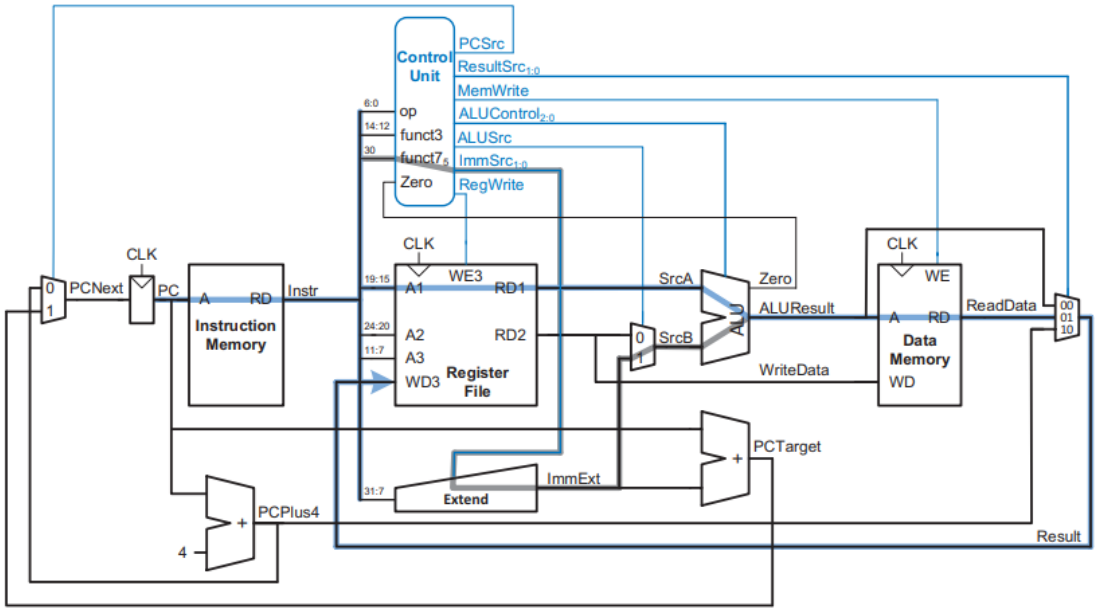
Theory/Description : The 32-bit RISC-V processor is based on the Reduced Instruction Set Computing (RISC) philosophy, which uses a simple and regular instruction format to improve efficiency, performance, and ease of hardware implementation. The RV32I base integer instruction set operates on 32-bit data and supports arithmetic, logical, memory access, and control flow instructions.

The processor is designed and implemented using Verilog HDL and consists of fundamental components such as the Program Counter (PC), Instruction Memory, Control Unit, Register File, Arithmetic Logic Unit (ALU), and Data Memory. The Program Counter sequentially fetches instructions from memory, while the Control Unit decodes the instruction and generates appropriate control signals. The ALU performs required computations based on the instruction type, and the Register File stores and retrieves operand values. For load and store operations, the Data Memory is accessed accordingly.

Overall, the processor follows the standard fetch-decode-execute cycle to process instructions while adhering to the RV32I architecture, ensuring correct functionality, modularity, and scalability.

Expected Outcome/outputs : Upon simulation of the 32-bit RISC-V processor in Verilog, the processor is expected to correctly fetch, decode, and execute instructions from the RV32I instruction set. The Program Counter should update sequentially (and change appropriately for branch and jump instructions), demonstrating correct control flow operation. The Register File should reflect correct data values after execution of arithmetic, logical, load, and store instructions. The ALU outputs should match the expected computational results based on the given instruction inputs. Performance and correctness can further be assessed by testing different instruction types, including R-type, I-type, S-type, B-type, and J-type instructions

Circuit Diagram(s) :



Block Diagram (s) :

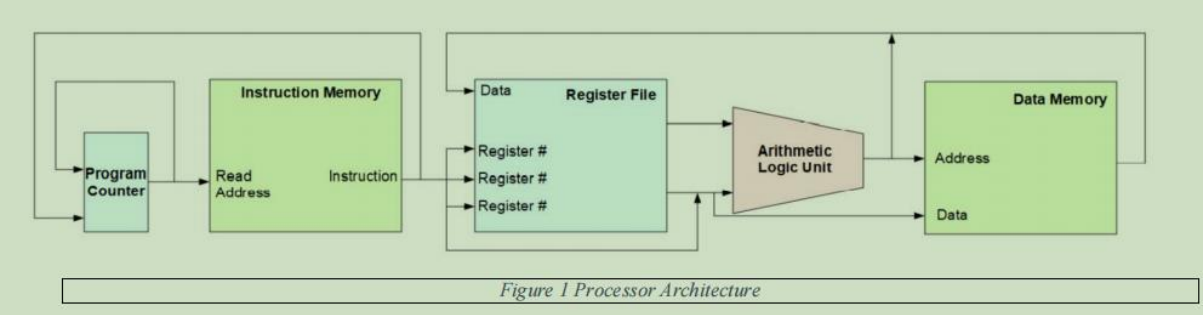
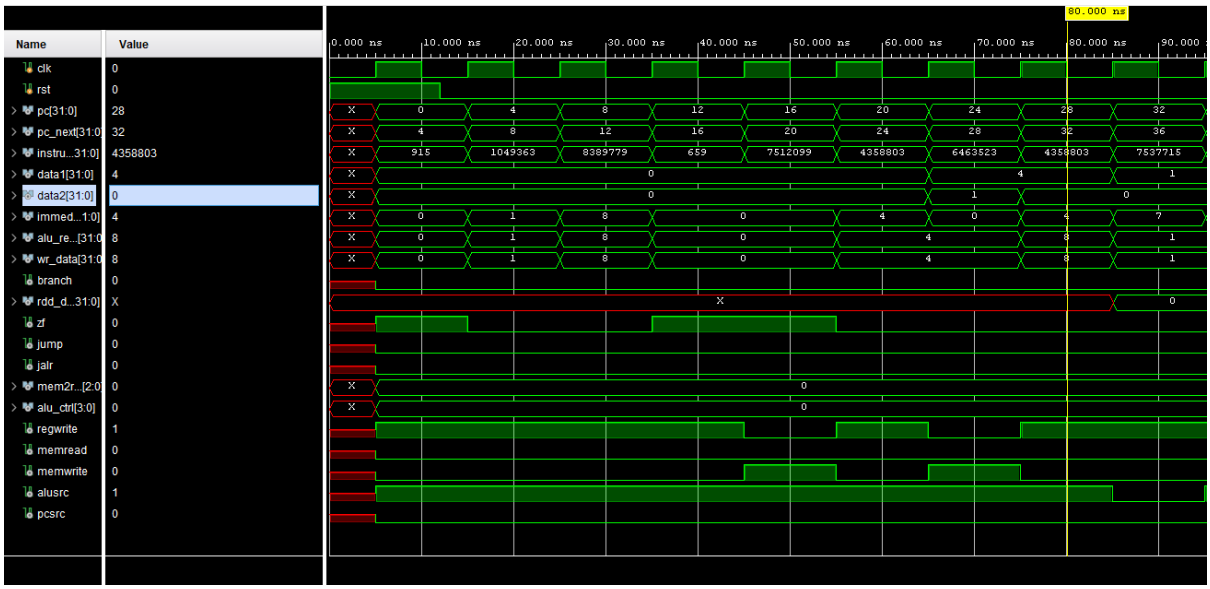


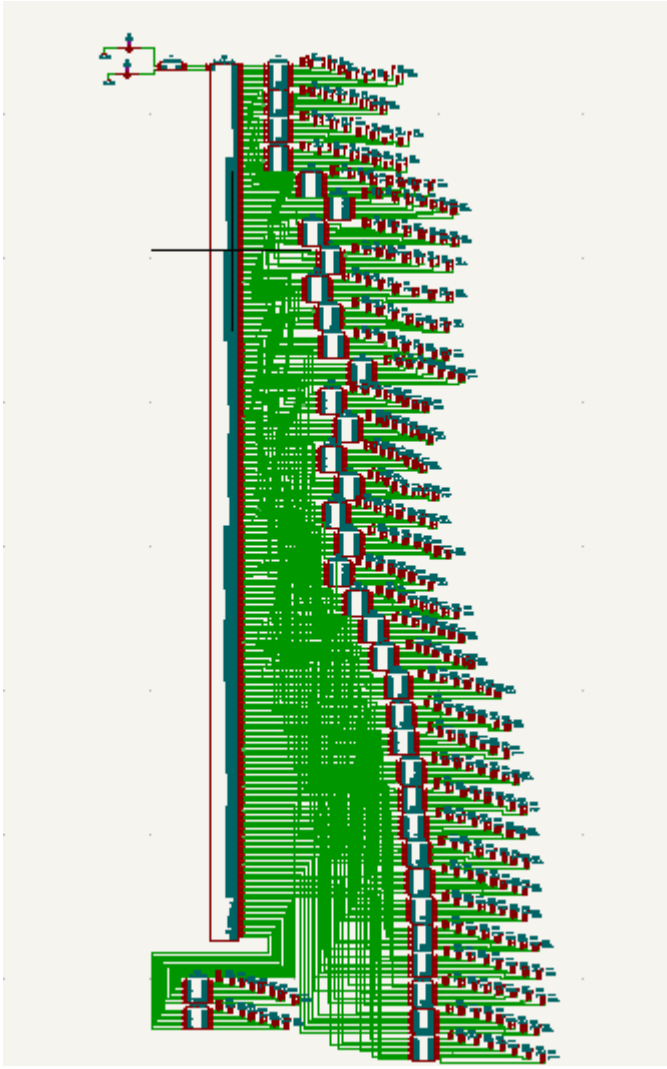
Figure 1 Processor Architecture

Expected Results (Input, Output waveforms and/or Multimeter readings) :

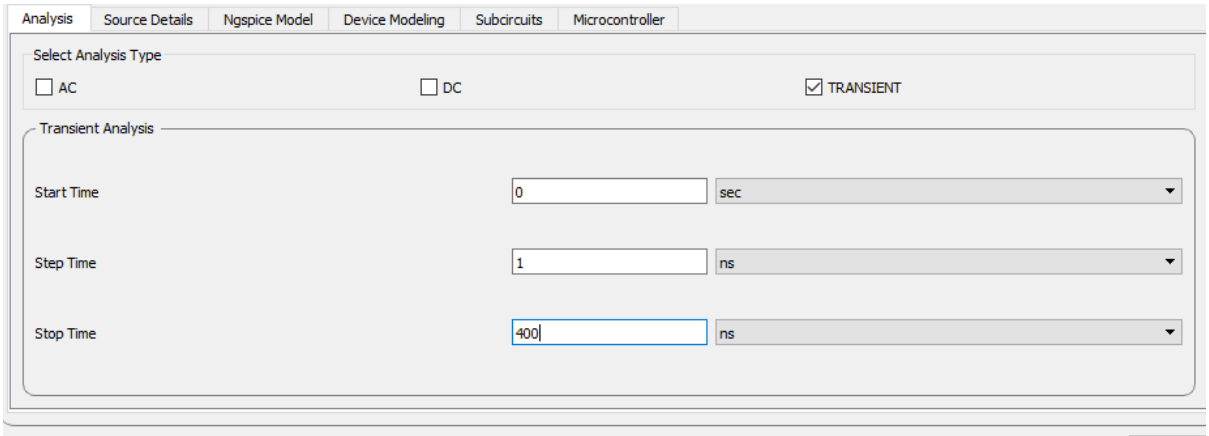


Circuit diagram :

Schematic :



Transient Analysis :



Clk Parameter :

Add parameters for pulse source v2

Enter initial value (Volts/Amps):	0
Enter pulsed value (Volts/Amps):	5
Enter delay time (seconds):	0
Enter rise time (seconds):	1n
Enter fall time (seconds):	1n
Enter pulse width (seconds):	5n
Enter period (seconds):	10n

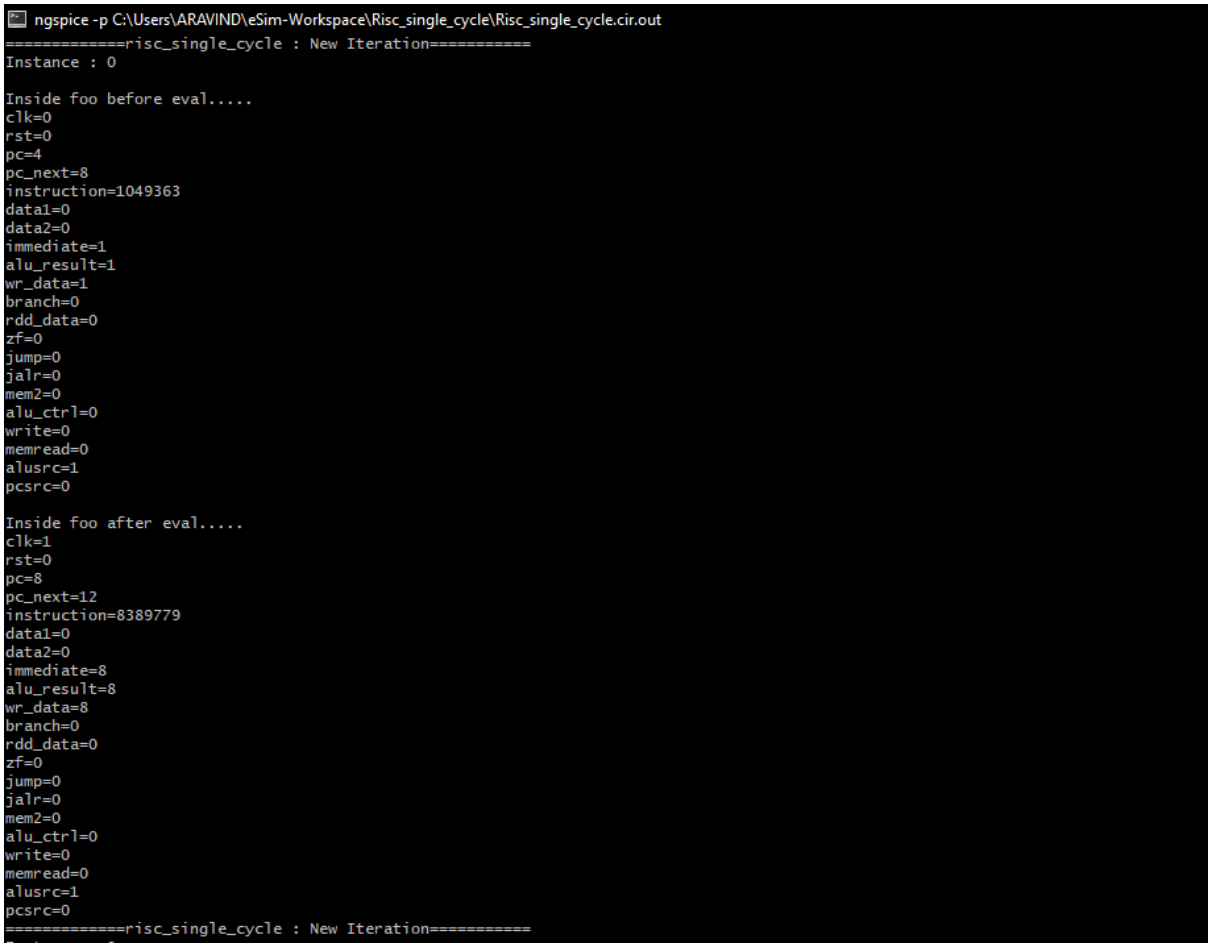
Rst parameter :

Add parameters for pulse source v1

Enter initial value (Volts/Amps):	5
Enter pulsed value (Volts/Amps):	0
Enter delay time (seconds):	20n
Enter rise time (seconds):	1n
Enter fall time (seconds):	1n
Enter pulse width (seconds):	0
Enter period (seconds):	0

Results :

The simulation shows correct sequential operation of the single-cycle RISC-V processor. The program counter increments by 4 each cycle, new instructions are fetched, and the ALU produces expected results based on the decoded instruction. This confirms proper instruction fetch, decode, and execution.



Research Paper/Journal/etc. :

Title : DESIGN OF 32 BIT RISC V PROCESSOR

Author : Meeradevi T,Mohanraj K,Mourissh B M

Link :https://ieeexplore.ieee.org/document/10726132

Source/Reference(s) :Digital Design & Computer Architecture RISC-V Edition