Simulation of a CMOS Low Dropout Voltage Regulator

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Abstract

Low Dropout Regulators (LDOs) are commonly used in modern integrated circuits to deliver stable, low-noise supply voltages even under varying load and input conditions. This work focuses on the design and simulation of a CMOS Low Dropout Regulator implemented in 180 nm technology, employing a two-stage error amplifier and a PMOS pass transistor. The regulator is designed to achieve stable operation, adequate loop gain, and reliable transient response while maintaining a low dropout voltage. All simulations are carried out using ngspice within the eSim environment. DC, AC, and transient analyses are performed to verify the functionality, stability, and regulation performance of the proposed LDO.

1 Theory and Description

The proposed Low Dropout Regulator (LDO) architecture is composed of four main functional blocks:

- Error Amplifier
- Miller Compensation Network
- PMOS Pass Transistor
- Resistive Feedback Network

The error amplifier is implemented as a two-stage CMOS amplifier. The first stage is a differential amplifier that compares the reference voltage (V_{ref}) with the feedback voltage (V_{FB}). Any difference between these two voltages is amplified and forwarded to the second stage. The second stage is a common-source amplifier, which provides additional gain and ensures effective driving of the PMOS pass transistor.

To ensure loop stability, a Miller compensation capacitor is connected between the intermediate node (V_x) and the output of the error amplifier ($V_{\text{OUT\_OPAMP}}$). This compensation technique introduces a dominant pole in the loop transfer function, thereby improving phase margin and stabilizing the feedback loop.

The PMOS pass transistor regulates the output voltage by controlling the amount of current delivered to the load. A resistive feedback divider samples the output voltage and feeds it back to the error amplifier, enabling closed-loop regulation and accurate control of the output voltage.

2 Circuit Diagram

The complete circuit schematic of the proposed LDO consists of the following key components:

- Differential input stage using NMOS transistors
- PMOS current mirror as active load
- Tail current source for biasing
- Second-stage common-source amplifier
- Miller compensation capacitor
- PMOS pass transistor
- Resistive feedback divider network

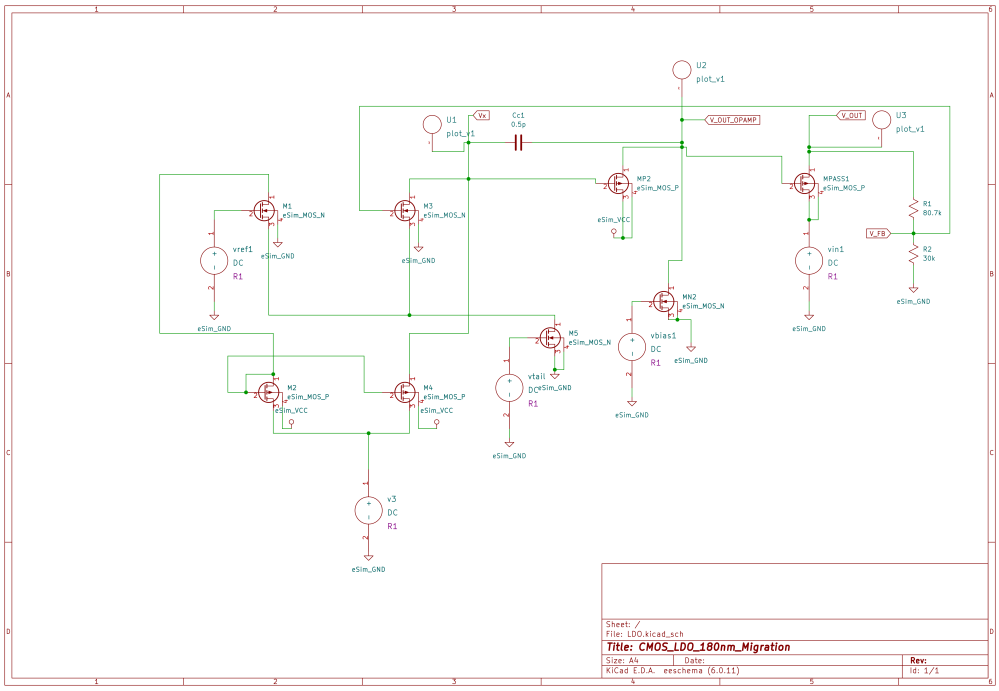

Figure 1: Schematic of the proposed CMOS Low Dropout Regulator

The entire circuit schematic is designed, implemented, and simulated using the eSim design environment, with ngspice employed as the simulation engine.

3 Results and Output

3.1 DC Analysis

The DC operating point analysis confirms that all transistors are properly biased in their intended regions of operation. The output voltage settles at the desired regulated value, indicating correct functionality of the LDO. Furthermore, the feedback voltage closely tracks the reference voltage, validating effective closed-loop regulation.

3.2 DC Sweep Analysis

The DC sweep analysis is performed by varying the reference voltage and observing the corresponding response of key node voltages in the LDO. Figure 2 shows the variation of the reference voltage (V_{ref}), feedback voltage (V_{FB}), and output voltage (V_{out}) with respect to the swept input.

It can be observed that the output voltage closely follows the reference voltage after the regulation point, indicating proper closed-loop operation. The feedback voltage tracks the reference voltage accurately, confirming correct operation of the resistive feedback network and the error amplifier. The deviation observed at lower sweep values corresponds to the dropout region, beyond which regulation is successfully achieved.

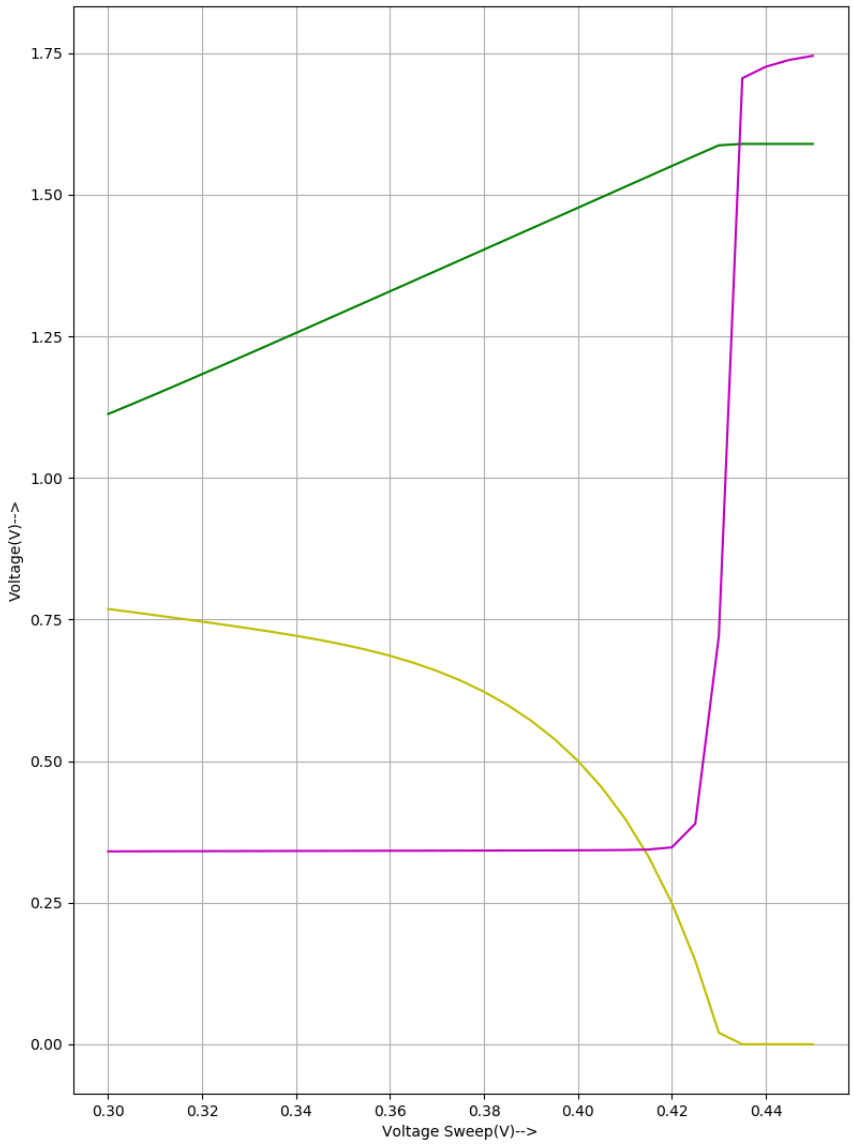

Figure 2: DC sweep showing reference voltage, feedback voltage, and regulated output voltage of the LDO

3.3 AC Analysis

AC analysis is performed to evaluate feedback loop stability. The compensated loop exhibits a dominant pole at the intermediate node, confirming the effectiveness of Miller compen-

sation. The loop exhibits a dominant pole with adequate phase margin, ensuring stable closed-loop operation.

3.4 Transient Analysis

Transient analysis is performed to evaluate the dynamic behavior of the LDO under time-varying conditions. Figure 3 illustrates the startup transient response of the regulator. The output voltage settles smoothly to the regulated value without overshoot or oscillations, indicating a stable startup behavior.

Figure 4 shows the load transient response of the LDO when a sudden change in load current is applied. A temporary dip in the output voltage is observed due to the abrupt load variation; however, the feedback loop quickly compensates for the disturbance and restores the output voltage to its nominal value. The absence of sustained oscillations confirms adequate phase margin and robust transient performance.

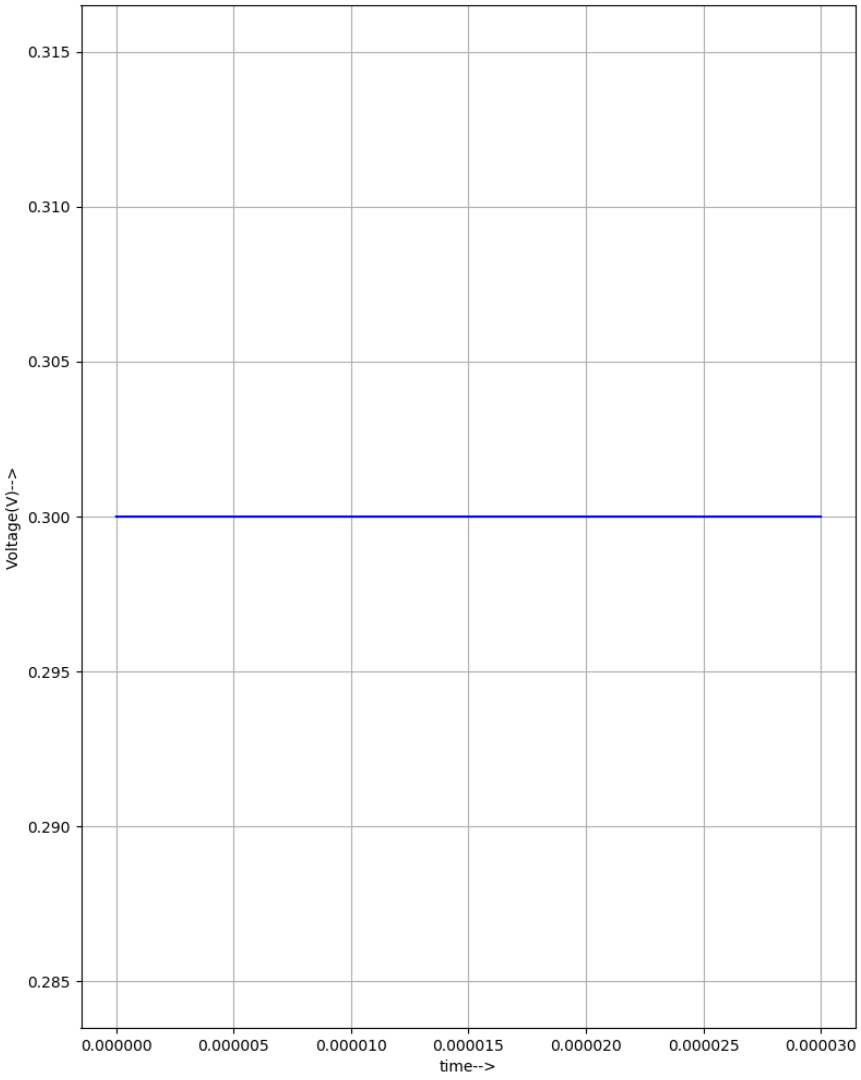

Figure 3: Startup transient response of the LDO output voltage

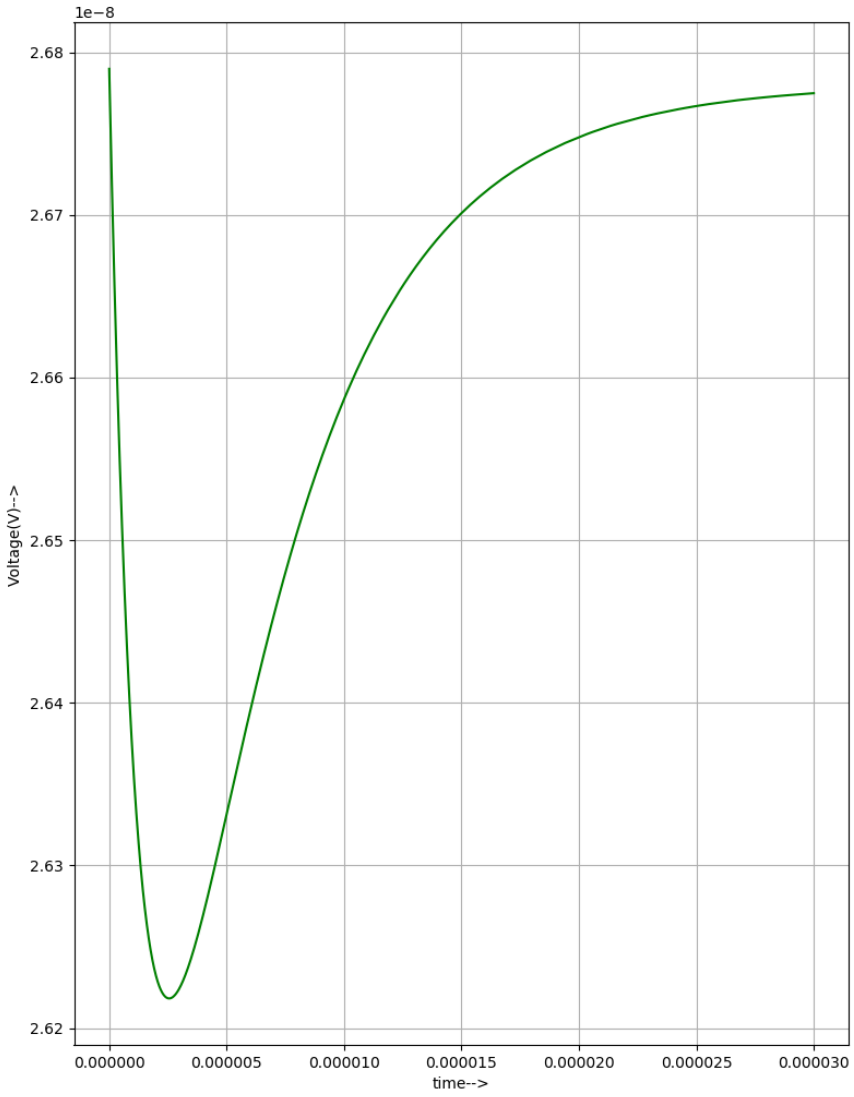

Figure 4: Load transient response of the LDO showing recovery after a sudden load change

4 Conclusion

The designed CMOS Low Dropout Regulator successfully achieves stable and reliable voltage regulation using a two-stage error amplifier with Miller compensation. Simulation results confirm proper DC operation, a stable frequency response, and robust transient behavior. Overall, the proposed LDO architecture is well suited for low-power integrated applications requiring dependable and efficient voltage regulation. The regulator is designed to deliver a

nominal output voltage of approximately 1.3 V from a 1.8 V supply while maintaining stable closed-loop operation.

5 References

References

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