Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

Name of the participant: Sufiyan Shaikh
Affiliation / Institution: Department of Electronics and Telecommunication Engineering, Pune Institute of Computer Technology, Pune, Maharashtra, India.

Title of the circuit: *Implementation of a Switched-Capacitor Low-Pass Filter Using an Op-Amp*

Theory/Description: A switched-capacitor (SC) low-pass filter is a discrete-time analog circuit that emulates the behaviour of a resistor using capacitors and electronic switches driven by a clock. The fundamental principle relies on periodic charge transfer rather than continuous current flow. When a capacitor is alternately connected between the input signal and a virtual ground node at a fixed clock frequency, it transfers a fixed amount of charge per cycle, resulting in an average current proportional to the input voltage. This behaviour is equivalent to a resistor whose value is defined by $R_{eq} = \frac{1}{Cf_{clk}}$.

In the implemented circuit, an operational amplifier is configured in an inverting topology with a switched capacitor acting as the effective input resistor and a fixed capacitor providing feedback. Non-overlapping clock signals control the analog switches, ensuring proper sampling, charge transfer, and reset of the switched capacitor in each clock cycle. The op-amp maintains a virtual ground at its inverting input, enabling accurate charge summation and stable operation. The resulting circuit functions as a low-pass filter whose cutoff frequency is determined by the ratio of the switched capacitor to the feedback capacitor and the clock frequency. High-frequency clock ripple is an inherent characteristic of switched-capacitor circuits and represents the discrete-time nature of operation.

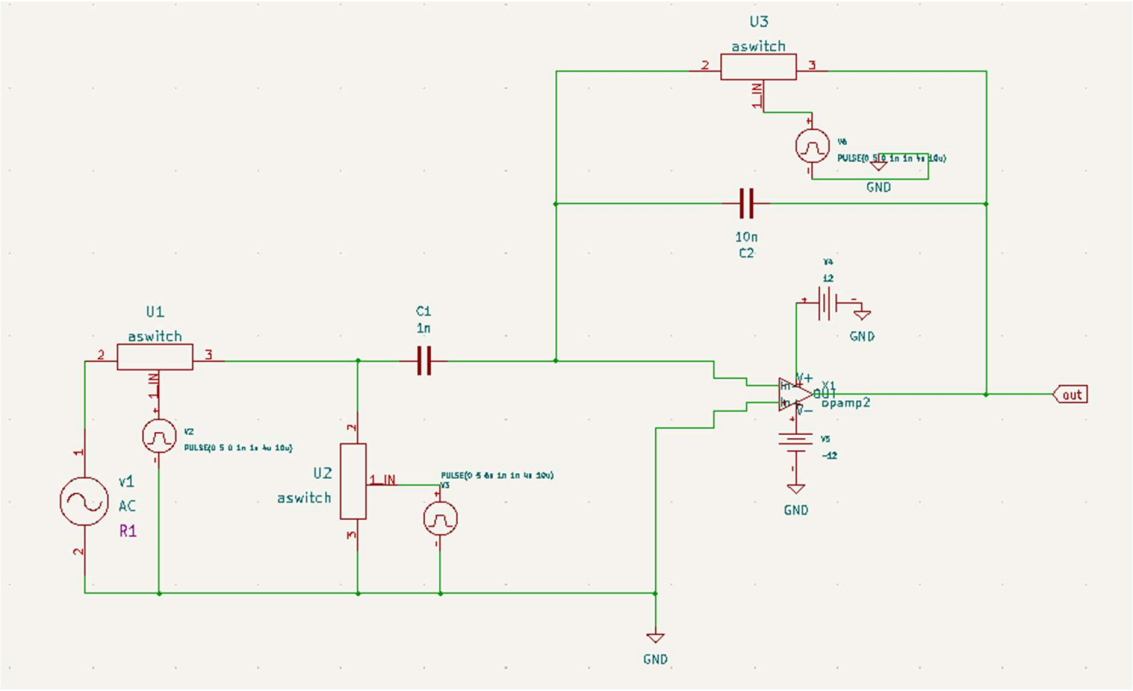
Reason to reproduce with eSim: This circuit is well suited for simulation using eSim as it is composed of standard SPICE-compatible components and relies primarily on transient analysis, which eSim efficiently supports. The open-source nature of eSim enables easy reproduction, modification, and verification of the circuit without the need for proprietary tools. The clear relationship between

theoretical operation and simulated results makes the circuit valuable for educational purposes and performance analysis, particularly for understanding clock-driven switched-capacitor systems.

Expected Outcome/outputs: When the circuit is simulated, it is expected to behave like a low-pass filter using switched-capacitor operation. The input signal is sampled using the clock-controlled switches, and the charge is transferred to the op-amp through the switched capacitor. As a result, the output follows the low-frequency variation of the input signal but also shows some high-frequency ripple due to the switching action, which is normal for switched-capacitor circuits.

The output signal is inverted, and its amplitude depends on the ratio of the switched capacitor and the feedback capacitor. The correct operation of the circuit can be verified by observing a stable output waveform without DC saturation and by checking that changes in clock frequency or capacitor values lead to expected changes in the filter response.

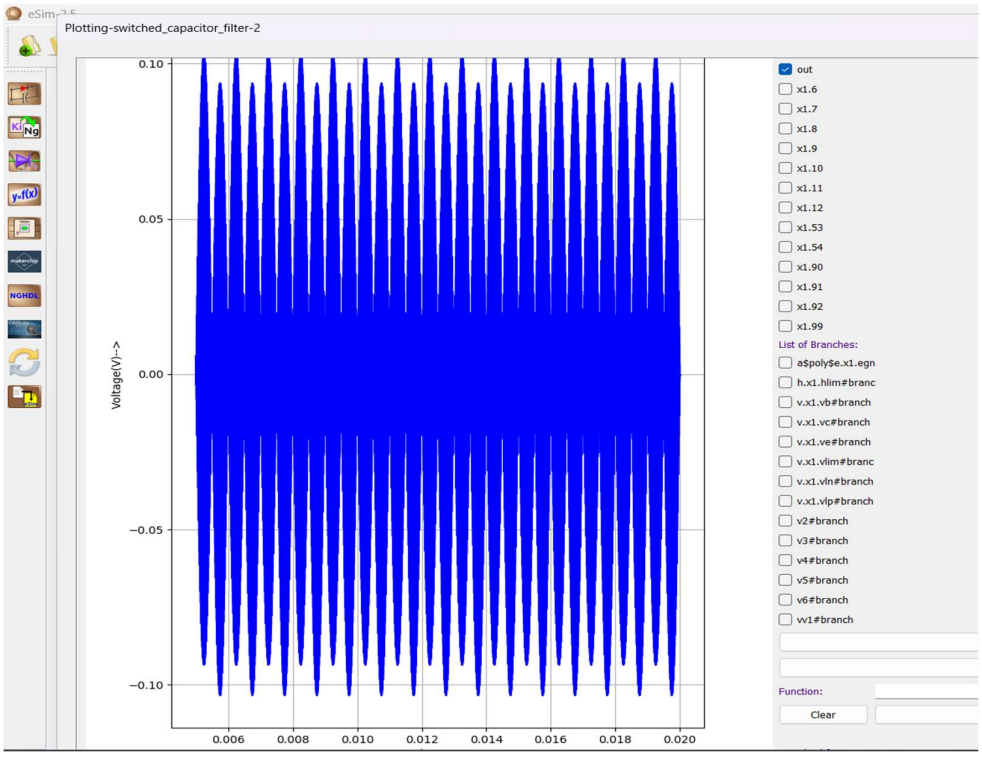
Circuit Diagram(s):

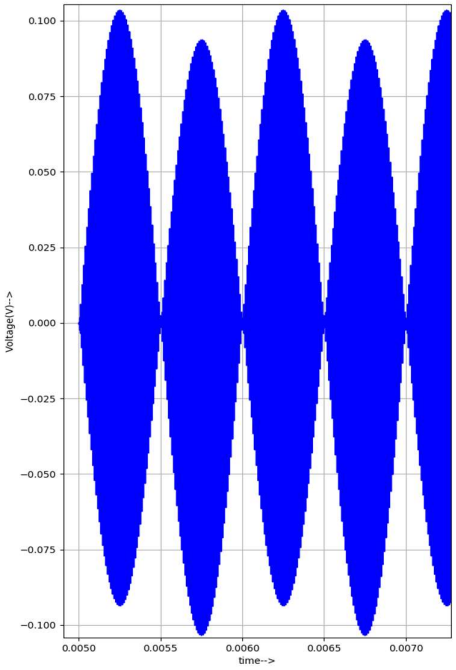


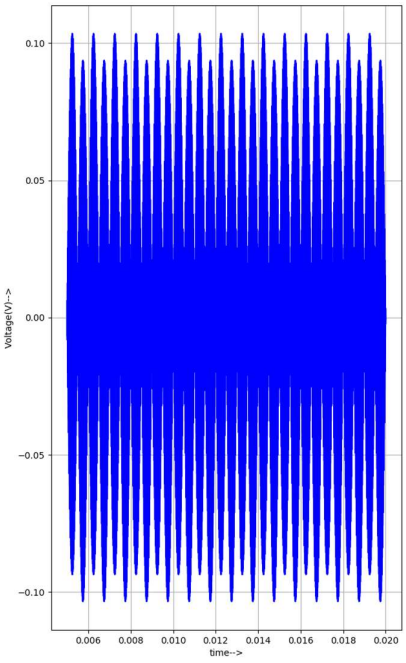
Results (Input, Output waveforms and/or Multimeter readings): The input to the circuit is a low-frequency sinusoidal voltage signal with a peak amplitude of approximately 100 mV and a frequency of 1 kHz. This input frequency is chosen to be much lower than the switching clock frequency of 100 kHz to ensure proper switched-capacitor operation and to avoid aliasing effects.

The simulated output waveform shows an inverted low-pass filtered version of the input signal. The output follows the low-frequency envelope of the input while exhibiting high-frequency ripple due to the clock-controlled switching action. This ripple is an inherent characteristic of switched-capacitor circuits and arises from discrete-time charge transfer at each clock cycle. The output amplitude remains bounded within approximately ±100 mV, indicating stable operation of the op-amp without saturation.

Initial transient behaviour is observed at the start of the simulation due to capacitor charging and op-amp settling. After this startup period, the circuit reaches steady-state operation, where the output waveform remains periodic and stable. Multimeter or probe measurements at the output node show an average voltage close to zero volts, confirming the absence of DC offset. Variations in clock frequency or capacitor values result in corresponding changes in the output response, validating the theoretical behaviour of the switched-capacitor low-pass filter.







Research Paper/Journal/etc.:

Title: Finite Amplifier Gain and Bandwidth Effects in Switched-Capacitor Filters
Author: G. C. Temes
Page No.: pp. 358–361
Link: https://ieeexplore.ieee.org/abstract/document/1051399

Source/Reference(s):

Textbook: *Design of Analog CMOS Integrated Circuits*
Author: Behzad Razavi
Publisher: McGraw-Hill
Relevance: This textbook was used to understand the fundamentals of switched-capacitor circuits, including switched-capacitor resistors, op-amp-based SC amplifiers, and non-overlapping clock operation.