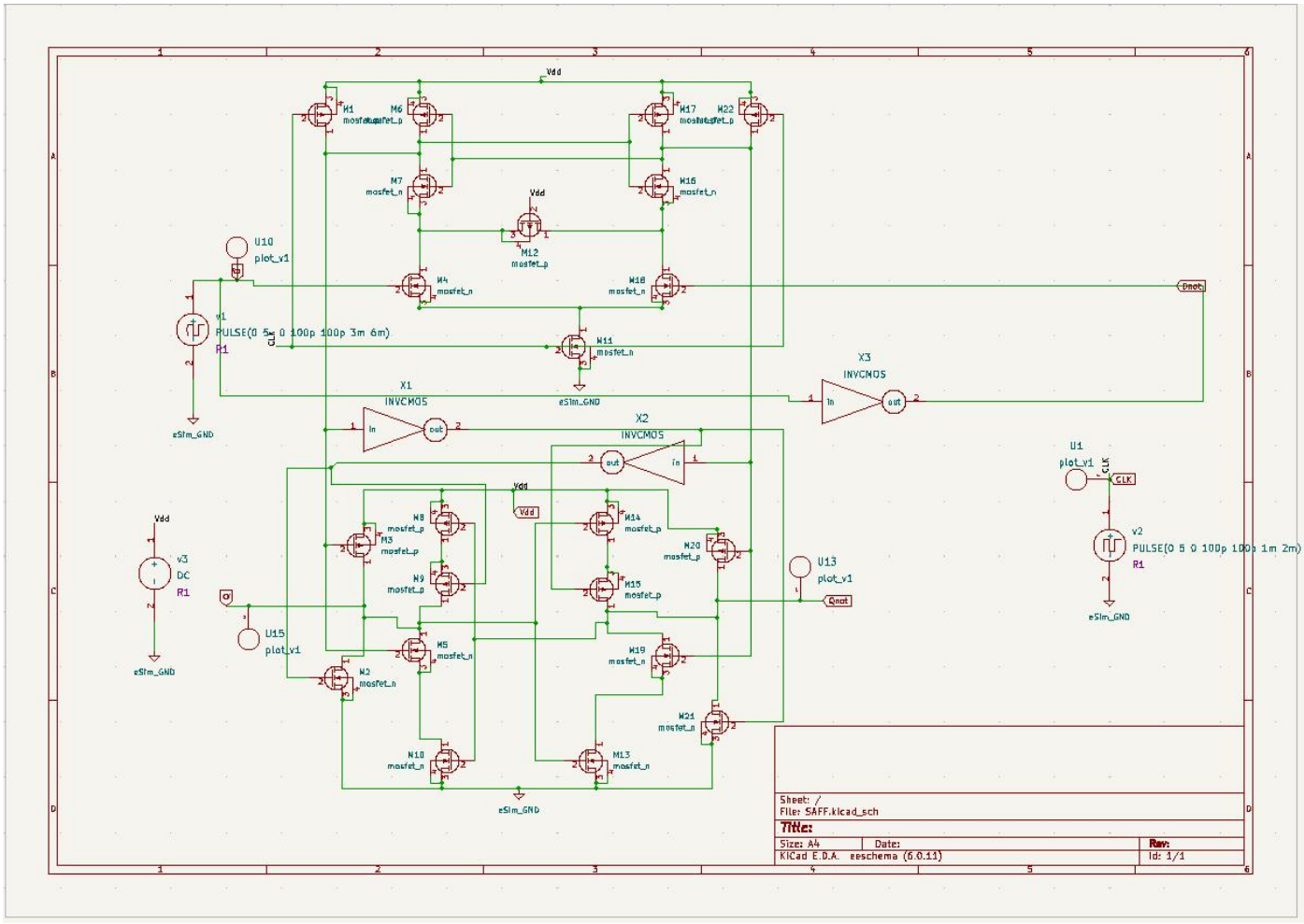
Title of the circuit : Low Noise, High accuracy Analog Electrocardiogram (ECG) Signal Front End Amplifier

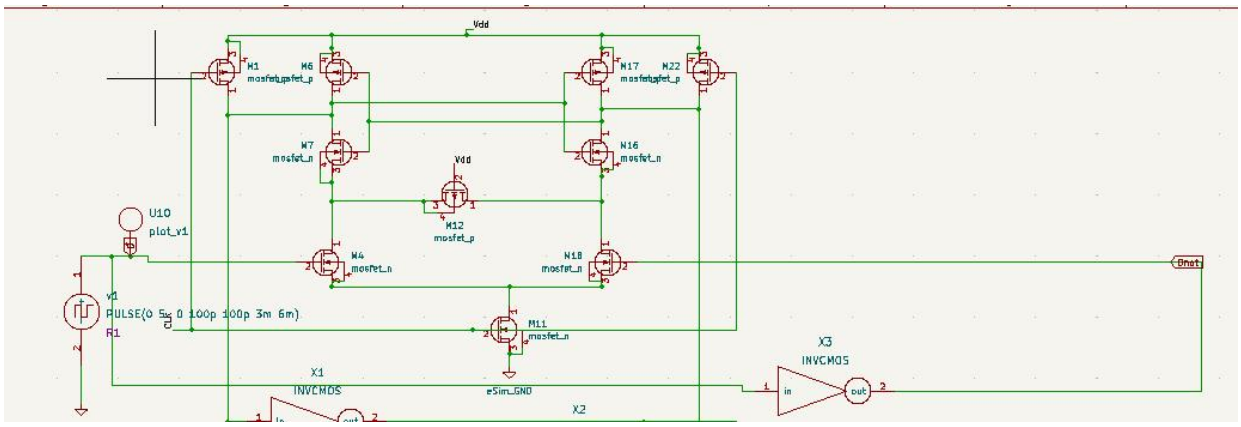
Theory/Description :

This circuit implements a modified Sense-Amplifier-Based Flip-Flop (SAFF) using CMOS transistors. The upper section forms the sense amplifier stage, which compares the differential input signals and generates a fast decision at the clock edge. The middle part consists of inverter buffers and control transistors that shape and stabilize the sensed signal. The lower section is the modified symmetric slave latch, which stores the sensed data and produces balanced Q and $\overline{Q}$ outputs with reduced delay. Overall, the circuit is designed to achieve high-speed, low-delay, and symmetric flip-flop operation suitable for high-performance digital systems.



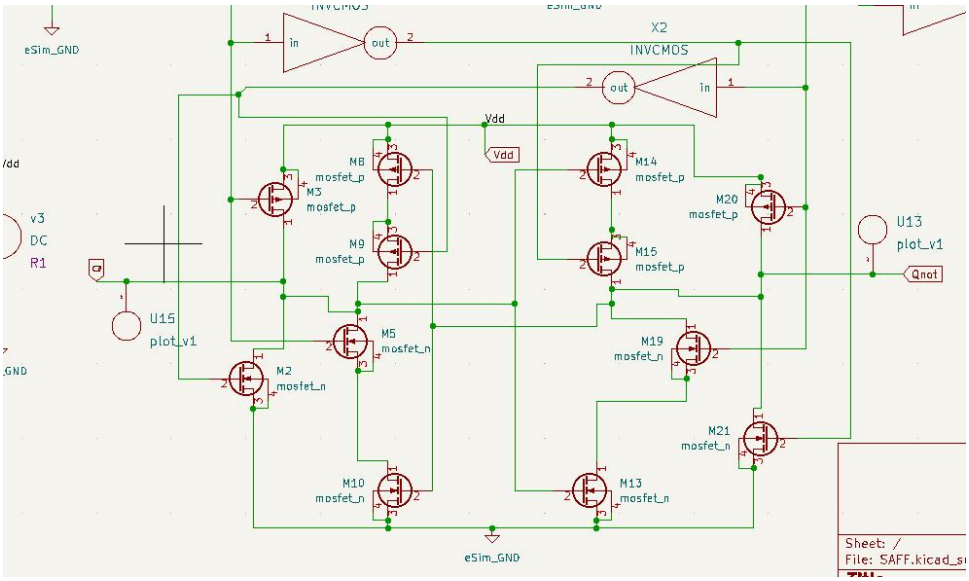
SENSE AMPLIFIER STAGE

The sense amplifier stage is the first part of the modified SAFF and is responsible for detecting and amplifying small differences between the input signals during the clock transition. It typically uses a differential pair of NMOS transistors with PMOS precharge devices, where internal nodes are precharged when the clock is low. When the clock goes high, the differential input causes one node to discharge faster than the other, creating a clear logic-level difference. This stage quickly converts the input data into a strong digital signal and isolates it from later changes in the input, ensuring fast and accurate data sensing for the flip-flop operation.



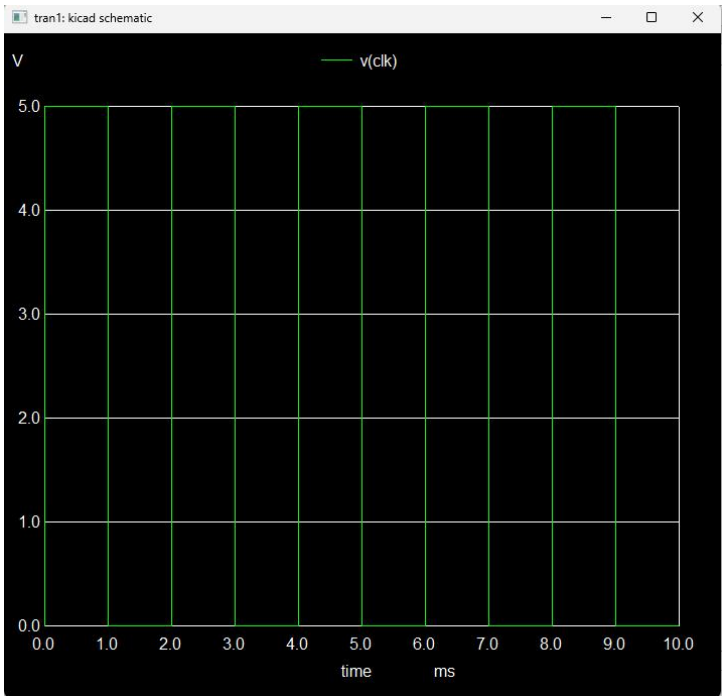
SLAVE LATCH STAGE

The second half of the modified SAFF is the slave latch stage, which stores the signal produced by the sense amplifier and generates the final outputs Q and $\bar{Q}$. Unlike the conventional SR latch, this stage uses a symmetric latch topology, so both output paths have similar transistor structures and delays. When the sense amplifier produces a pulse at the clock edge, the latch captures this change and holds the corresponding logic state until the next clock cycle. This design reduces propagation delay, improves output balance, and increases driving capability, resulting in faster and more reliable flip-flop operation.

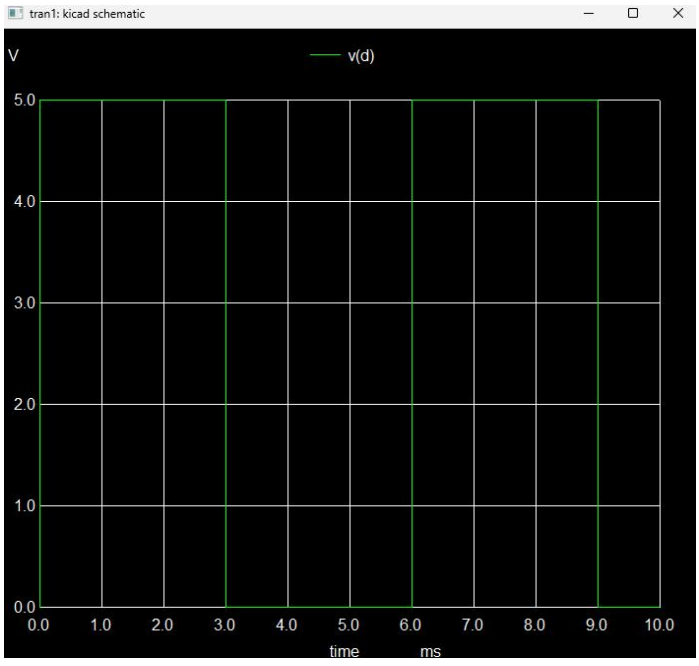


INPUT SIGNAL WAVEFORM:

CLK

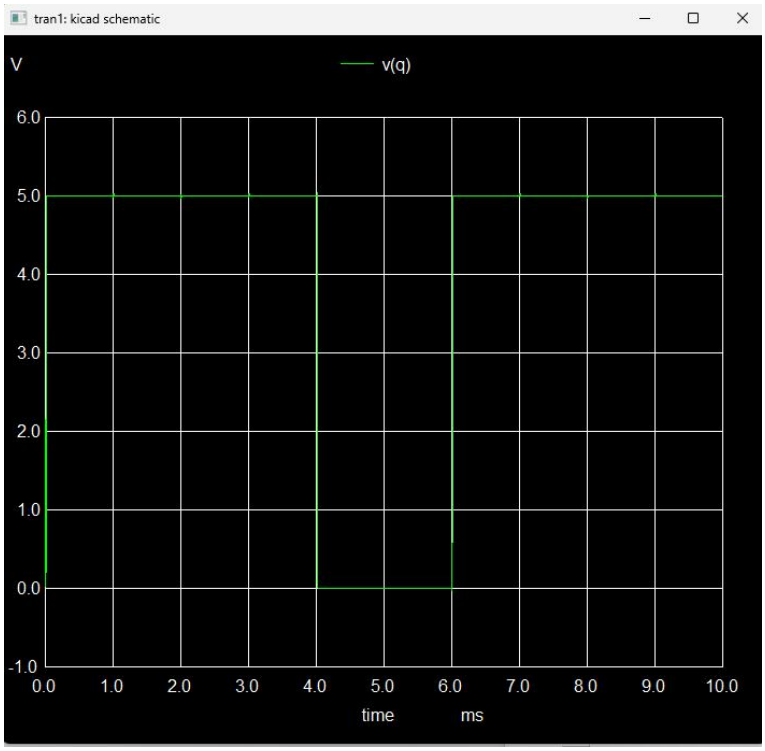


D

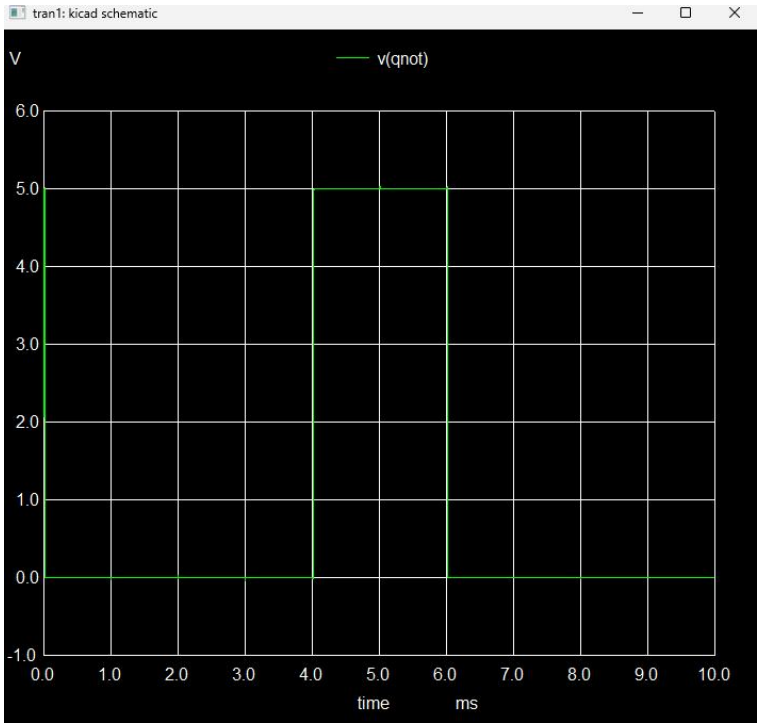


OUTPUT SIGNAL WAVEFORM:

Q



Q’



It typically shows the waveforms of CLK (clock), D (input), Q, and $\overline{Q}$ (outputs). When the clock edge occurs, the flip-flop samples the input D, and the output Q changes accordingly while $\overline{Q}$ shows the complementary value. The graph also illustrates the timing behavior of the circuit, such as clock-to-Q delay, setup time, and hold time, and demonstrates that the modified SAFF produces faster and more symmetric output transitions compared to the conventional design

SOURCE/REFERENCE:

Improved Sense-Amplifier-Based Flip-Flop: Design and Measurements Borivoje Nikolic´, Member, IEEE, Vojin G. Oklobdzija ˇ , Fellow, IEEE, Vladimir Stojanovic´, Wenyan Jia, Member, IEEE, James Kar-Shing Chiu, and Michael Ming-Tak Leung

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