Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit: Design and Simulation of a Transmission-Gate Based Edge-Triggered CMOS D Flip-Flop Using eSim

Theory/Description: Flip-flops are fundamental building blocks in digital and VLSI systems, widely used in registers, counters, pipelines, and memory elements. Among various types of flip-flops, the edge-triggered D flip-flop is preferred due to its predictable timing behaviour and reliable data storage. An edge-triggered flip-flop captures the input data only at a specific clock edge, thereby avoiding race conditions and glitches associated with level-sensitive circuits.

In CMOS VLSI design, transmission-gate based flip-flops are commonly used because of their low power consumption, full voltage swing, and improved noise margins. A transmission gate consists of parallel NMOS and PMOS transistors controlled by complementary clock signals, allowing bidirectional signal transfer with minimal signal degradation. By combining transmission gates with inverters, a master–slave configuration can be formed to achieve edge-triggered operation. In a transmission-gate based edge-triggered CMOS D flip-flop, two latches are connected in series. The master latch samples the input data when the clock is in one phase, while the slave latch holds the data during the opposite phase. This arrangement ensures that the output changes only at the clock edge, making the circuit suitable for synchronous digital systems.

In this proposed work, a transmission-gate based edge-triggered CMOS D flip-flop will be designed and simulated using eSim. The operation of the flip-flop will be verified through transient analysis by applying clock and data signals, and the correct edge-triggered behaviour will be observed at the output.

Reason to reproduce with eSim: Most transmission-gate based CMOS flip-flop designs reported in textbooks and research literature are simulated using proprietary EDA tools. This limits access for students and researchers who rely on open-source software. Reproducing a transmission-gate based edge-triggered CMOS D flip-flop using eSim provides an open-source platform for studying sequential logic at the transistor level.

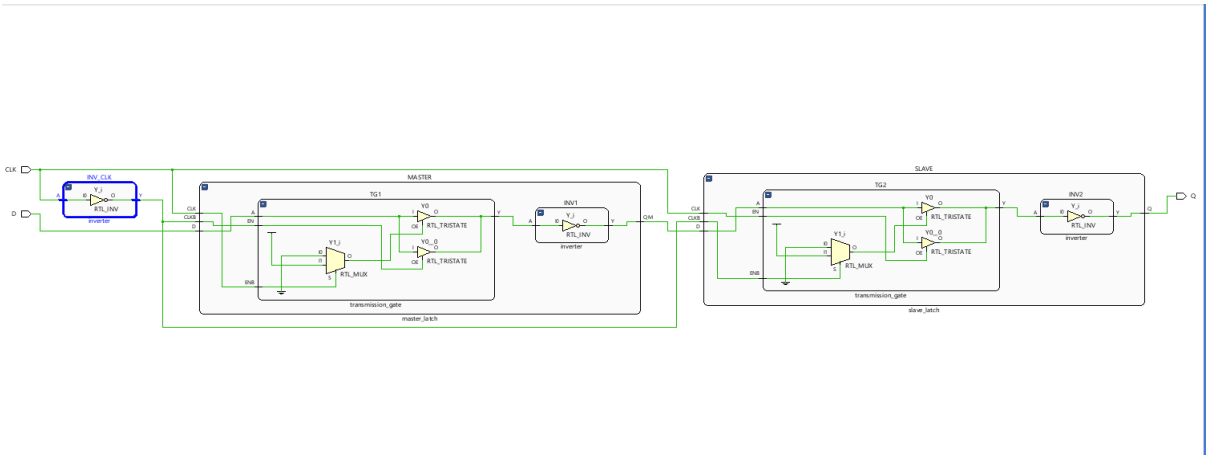
Migrating this circuit to eSim helps validate the capability of eSim and ngspice in handling CMOS sequential circuits and clocked behaviour. This work will be beneficial for students learning VLSI design, as it allows them to understand internal transistor-level operation rather than abstract behavioural models. The availability of such a circuit in eSim also contributes to building a reusable open-source repository of standard VLSI building blocks for academic and research purposes.

Expected Outcome/outputs:

- Successful design of a transmission-gate based edge-triggered CMOS D flip-flop using eSim
- Verification of correct edge-triggered operation through transient simulation
- Observation of correct data transfer from input (D) to output (Q) on the active clock edge
- Demonstration of stable output storage during inactive clock periods
- Clear understanding of CMOS transmission-gate based sequential circuit behaviour

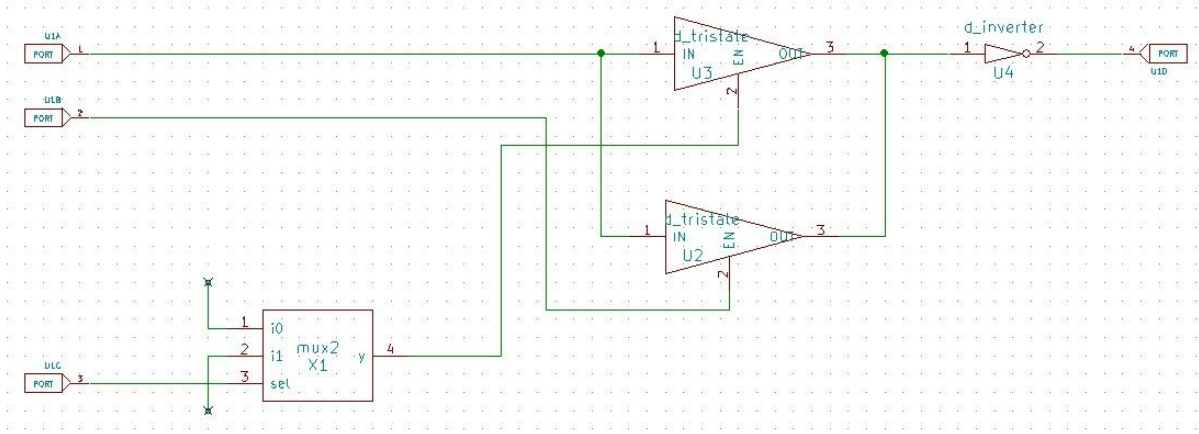
Circuit Diagram(s): The circuit diagram consists of CMOS transmission gates implemented using NMOS and PMOS transistors, combined with inverters to form a master–slave latch configuration. Complementary clock signals are used to control the transmission gates and achieve edge-triggered operation. The schematic is based on standard CMOS transmission-gate flip-flop designs reported in literature.

Schematic Diagram:



Img 1: Schematic Diagram

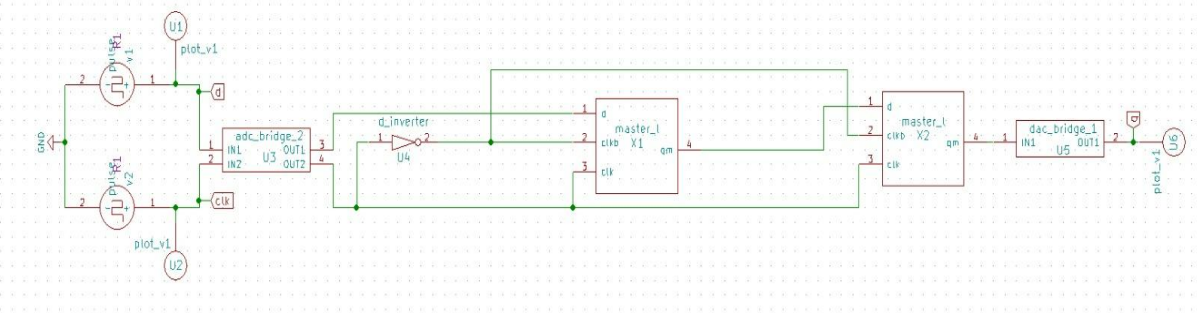
Expected Results (Input, Output waveforms and/or Multimeter readings): When a clock signal and data input are applied, the output is expected to change only at the triggering edge of the clock. Transient simulation results will show that the output follows the input data at the clock edge and remains stable during the rest of the clock cycle. This confirms correct edge-triggered flip-flop operation.



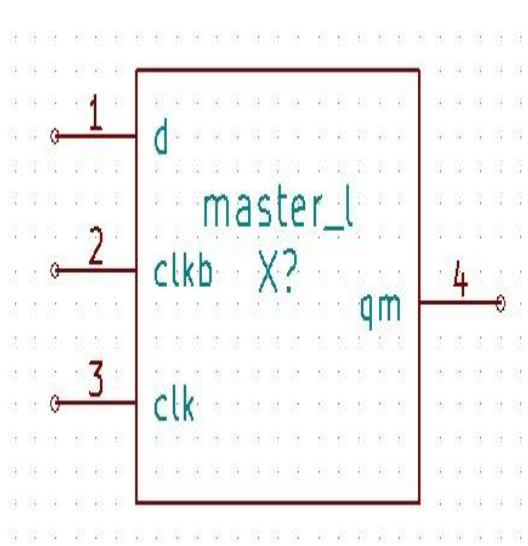
Img 2: Master Latch schematic diagram

Test Circuit:

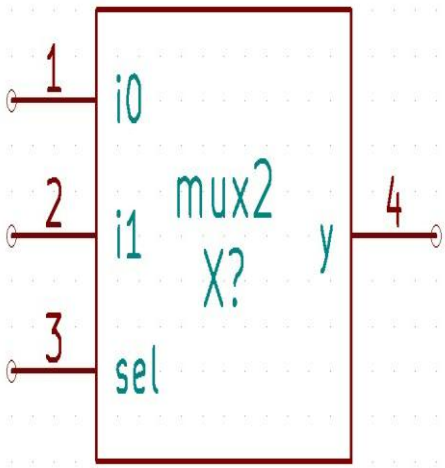
The test circuit is designed to verify the operation of the transmission-gate based edge-triggered CMOS D flip-flop through simulation. A clock signal and varying data inputs are applied to the circuit, and the output is observed at each clock edge. The simulation confirms that the output updates only on the active clock edge and holds its previous value otherwise. The observed waveforms are compared with the expected D flip-flop behavior to validate correct edge-triggered operation and proper data storage.



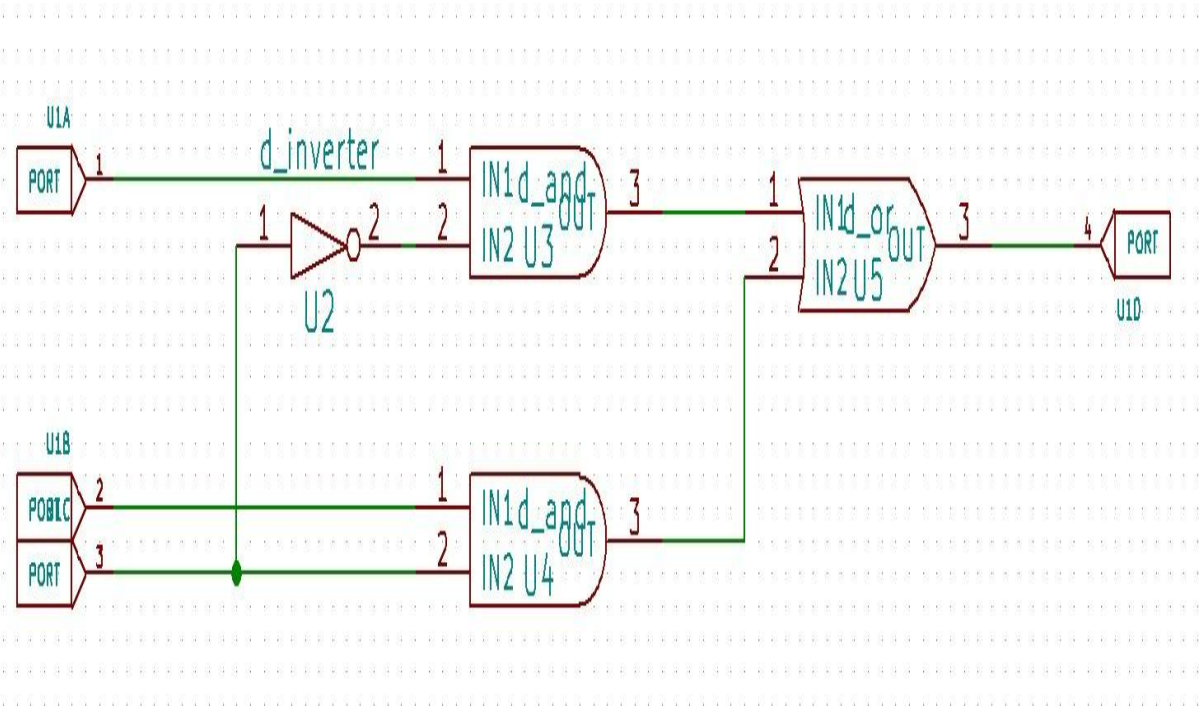
Img 3: Test Circuit



Img 4: Master subcircuit

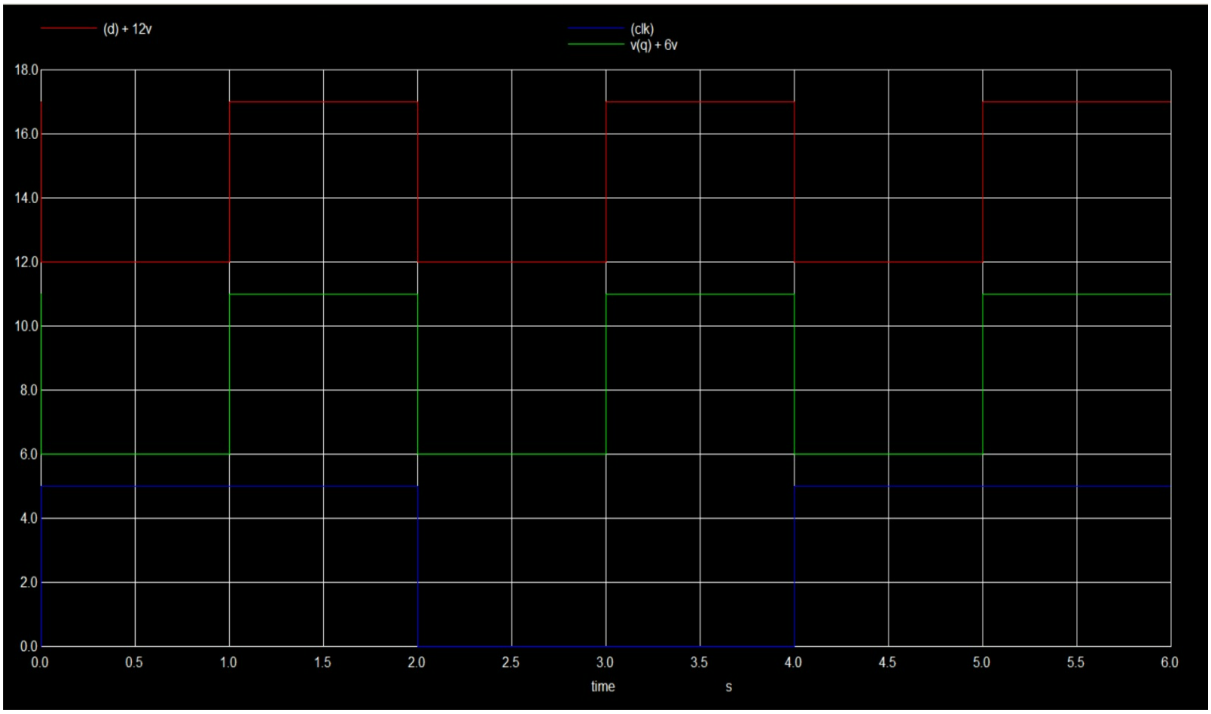


Img 5: Mux subcircuit



Img 6: Mux schematic diagram

Simulation Output:



Img 7: Output Graph

Truth Table:

Truth Table – Edge-Triggered D Flip-Flop

Clock (CLK)	Data (D)	Output Q (Next State)	Explanation
↑ (Rising edge)	0	0	On rising edge, Q captures D = 0
↑ (Rising edge)	1	1	On rising edge, Q captures D = 1
0	X	Q (previous)	No clock edge → output holds value
1	X	Q (previous)	No clock edge → output holds value
↓ (Falling edge)	X	Q (previous)	Output does not change on falling edge

Research Paper/Journal:

Title: CMOS VLSI Design: A Circuits and Systems Perspective
Author: Neil H. E. Weste, David Harris
Page No.: Chapter on Sequential Logic and Flip-Flops
Link: https://ieeexplore.ieee.org/document/133185

Source/Reference(s):

1. Neil H. E. Weste and David Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Pearson Education.
2. R. J. Baker, *CMOS Circuit Design, Layout, and Simulation*, Wiley Publications.
3. eSim Official Documentation – https://esim.fossee.in
4. Ngspice User Manual – https://ngspice.sourceforge.net
