Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit : **Design and Analysis of a Dual-Mode Approximate 4-Bit Adder for Low-Power Applications**

Theory/Description :

A 4-bit ripple carry adder adds two 4-bit binary operands and produces a 4-bit result along with a carry-out bit. The conventional ripple carry adder consists of four full adders connected in series, where the carry output from one stage becomes the carry input for the next. While this design is functionally accurate, it suffers from high propagation delay and increased power consumption due to carry propagation through all stages.

In the dual-mode approximate adder, the adder operates in two selectable modes:

- Accurate Mode: Functions as a standard ripple carry adder, with correct carry propagation through all bits.
- Approximate Mode: Simplifies the carry propagation by bypassing or disabling carry generation from the least significant bits. This reduces switching activity, propagation delay, and dynamic power consumption. The approximation introduces a controlled error that is acceptable in many real-world applications like image/video processing, sensor data accumulation, and AI/ML accelerators.

The dual-mode operation is controlled by a MODE input signal. When MODE is logic ‘0’, the adder behaves accurately; when MODE is logic ‘1’, carry propagation from lower bits is limited to reduce circuit activity. This improves performance metrics at the expense of a small degradation in numerical precision.

Reason to reproduce with eSim :

Reproducing the dual-mode approximate adder in eSim aligns with the objective of open-source digital circuit design and analysis. The circuit demonstrates trade-offs between accuracy and power/delay performance, which is a fundamental aspect of low-power digital

design. Using eSim's transistor-level environment backed by Ngspice simulation, an accurate evaluation of switching activity, propagation delay, power consumption, and output correctness can be performed without relying on proprietary tools. Additionally, such a design enhances the repertoire of digital circuit examples in eSim, encouraging the adoption of open-source EDA tools in academia and research.

Expected Outcome/outputs :

- Correct simulation of the 4-bit adder in both Accurate Mode (MODE=0) and Approximate Mode (MODE=1)
- Transient output waveforms showing:
    - Sum outputs S0–S3 and Carry Out in both modes
    - Reduced delay in approximate mode compared to accurate mode
- Power analysis data showing:
    - Lower dynamic power consumption in approximate mode
- Tabulated comparison of:
    - Delay (propagation time)
    - Power
    - Error rate (difference between accurate and approximate outputs)
- Demonstration of controlled error (limited error magnitude) in approximate mode

Circuit Diagram :

1. 4-bit Adder Block

- Four full adders (FA0, FA1, FA2, FA3)
- Each FA implemented using CMOS logic gates
- Carry out of each stage connects to carry in of next stage

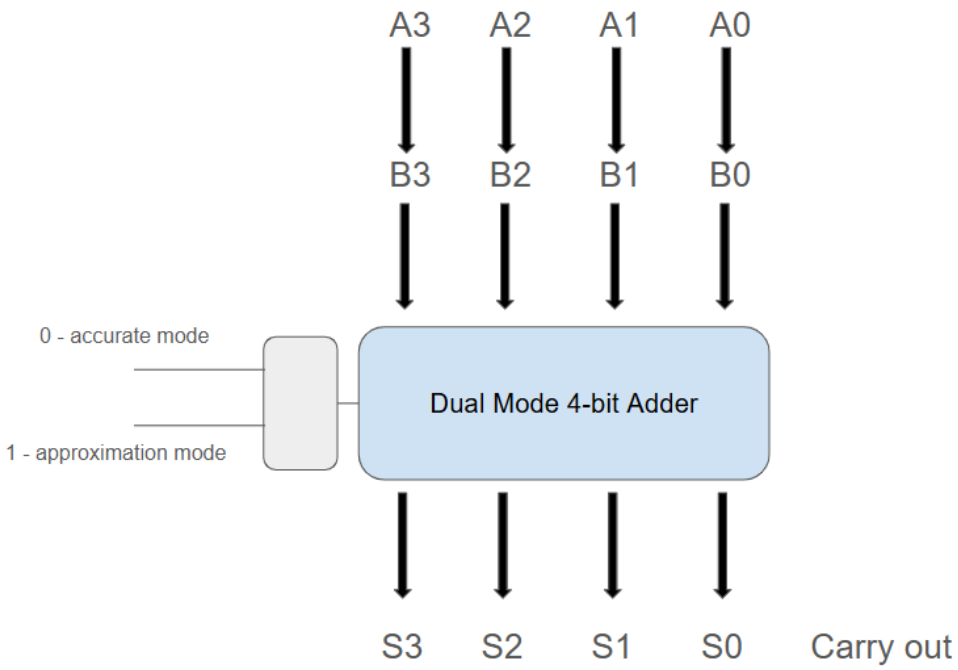
2. Approximation Logic

- MODE signal controls whether carry from FA0 (and optionally FA1) is passed forward
- When MODE=1 (approximate), the carry from FA0 is forced to 0 (or selectively bypassed)
- Multiplexer (2:1) can be used to select between accurate and forced carry signal

3. Control Block

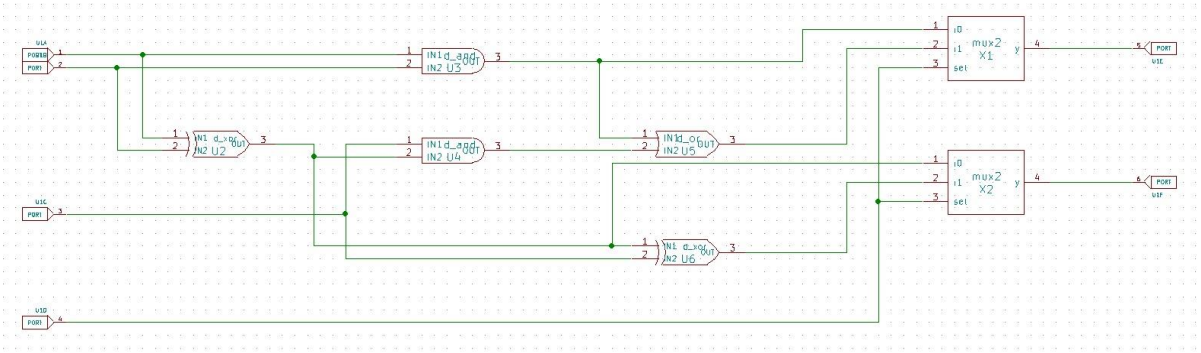
- One MODE input
- MUX selects carry enable path

Block Diagram :

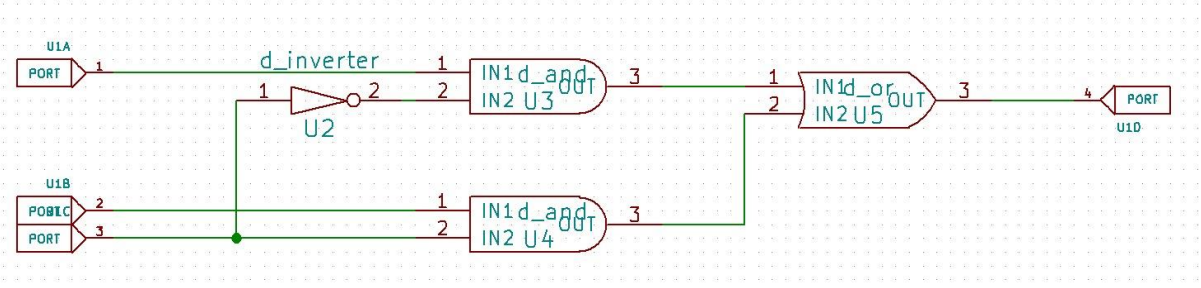


Img 1 : Block Diagram

Schematic Diagram :

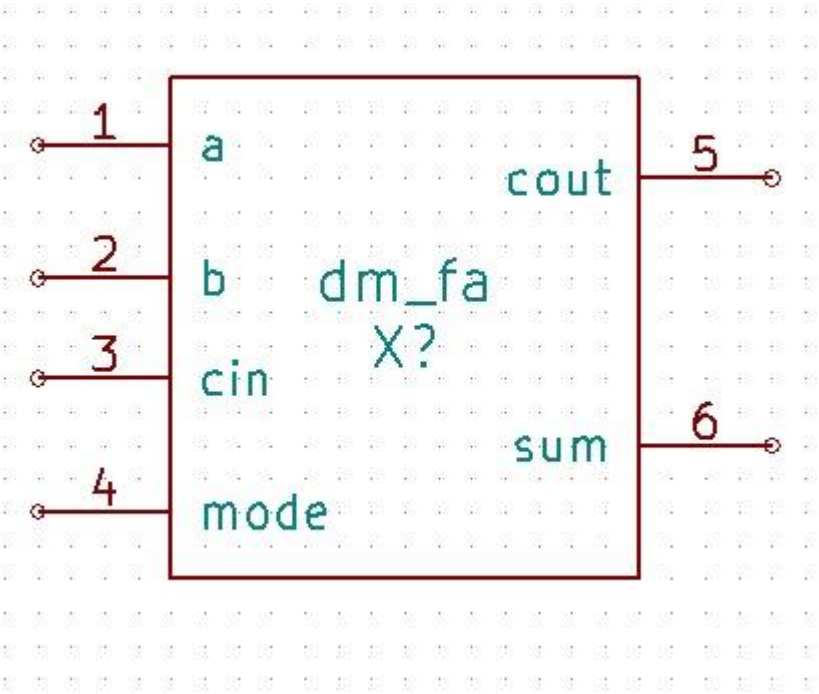


Img 2 : Full Adder schematic diagram

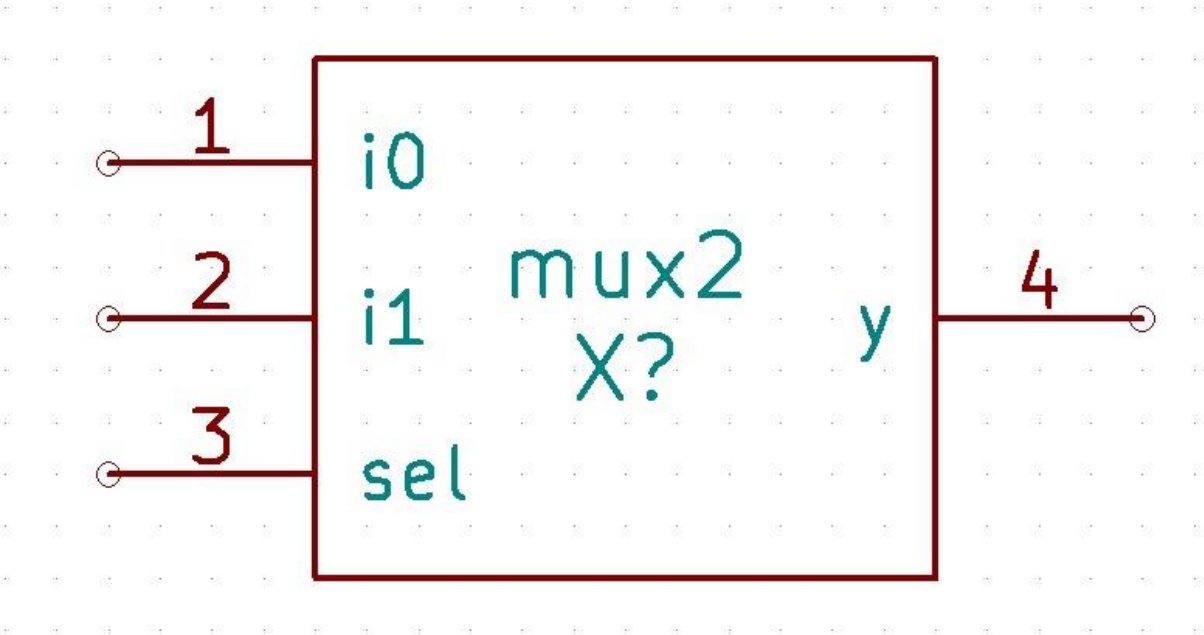


Img 3 : Multiplexer schematic diagram

Subcircuit Diagram :

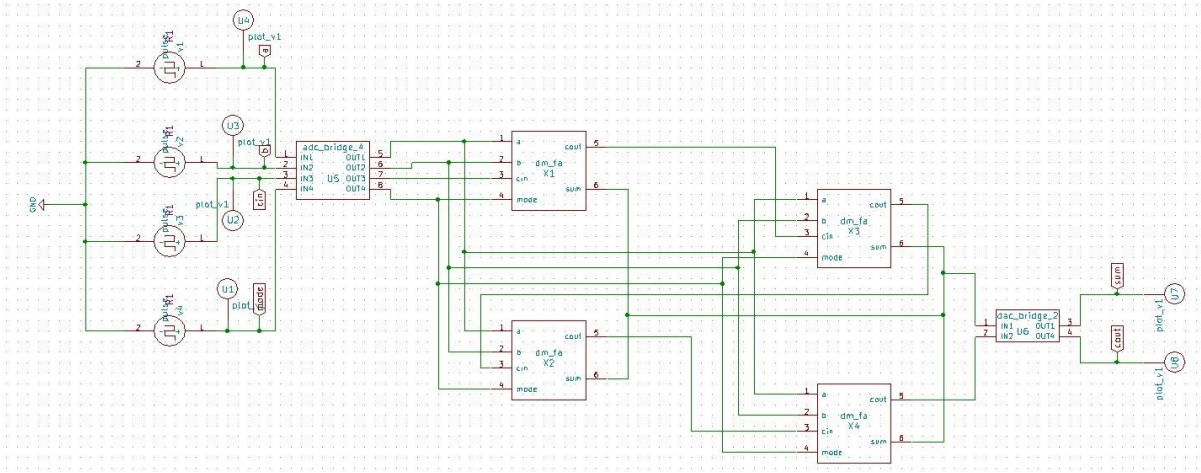


Img 4 : Full adder subcircuit



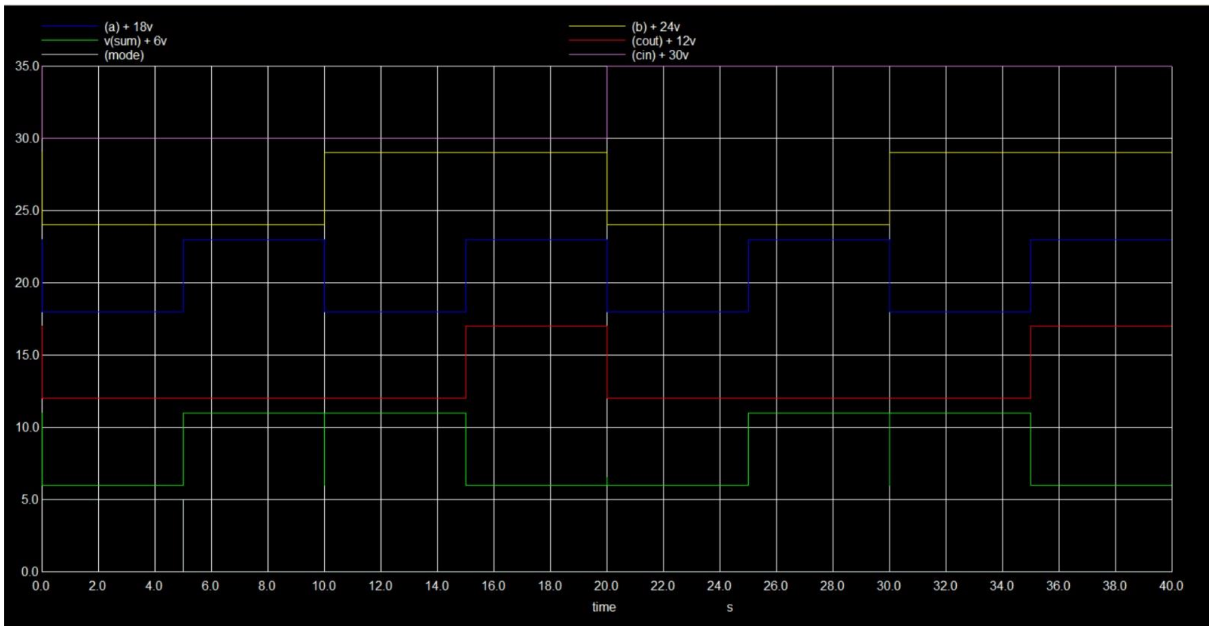
Img 5 : Multiplexer subcircuit

Test Circuit :



Img 6 : Test circuit

Simulation Output :



Img 7 : Simulation output

Truth Table :

MODE	A	B	Cin	Sum	Cout
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1

0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	1	0
1	0	1	1	1	0
1	1	0	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1
1	1	1	1	0	1

Research Paper/Journal/etc. :

Title : Low-Power Digital Signal Processing Using Approximate Adders

Author : Vaibhav Gupta, Debabrata Mohapatra, Anand Raghunathan, Kaushik Roy

Journal : IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems

Year : 2013

Volume : 32, Issue : 1, Pages : 124–137

Link : https://ieeexplore.ieee.org/document/6394123

Source/Reference(s) :

1. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems – foundational journal for approximate arithmetic research.

2 Approximate Arithmetic Circuits survey (University PDF) – comprehensive survey of design methods and metrics.

3. eSim / Ngspice documentation for simulation setup and power analysis.