Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit : 4-Bit Gray Code to Binary Code Converter

Theory/Description : The Gray code is a binary numeral system in which consecutive numbers differ by only one bit, reducing the chances of errors during digital transitions. This circuit converts a 4-bit Gray code input into its equivalent binary code output using combinational logic. The conversion is performed using cascading XOR gates. Specifically, the most significant binary bit (B3) is equal to the most significant Gray code bit (G3), and each subsequent binary bit is obtained by XOR-ing the previous binary bit with the corresponding Gray code bit. This purely digital circuit involves AND, OR, XOR, and NOT gates.

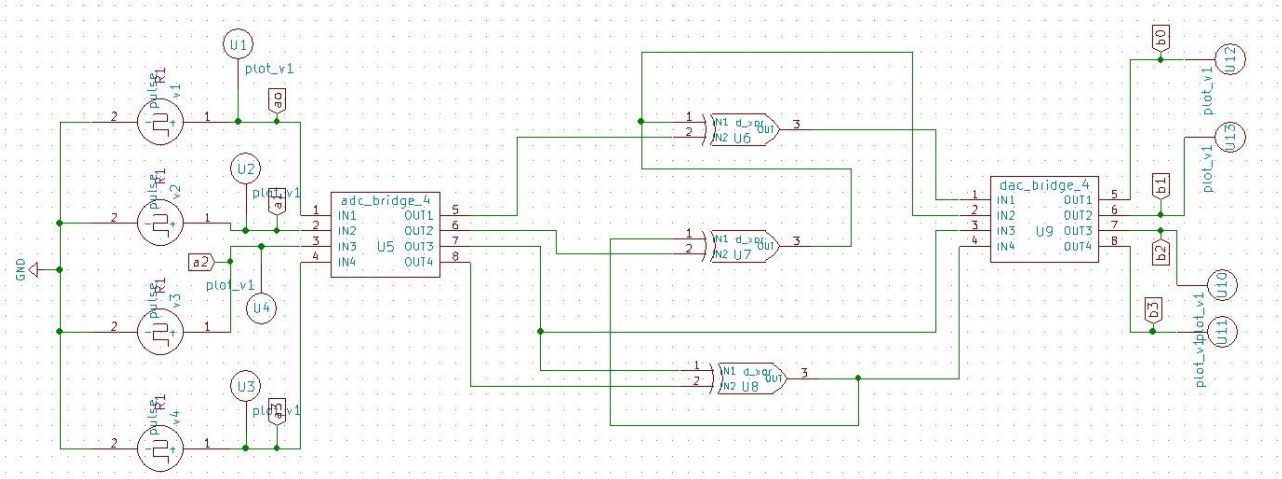
Reason to reproduce with eSim : This circuit is ideal for simulation in eSim because it demonstrates the design and verification of combinational digital circuits. Using eSim, the circuit can be simulated and validated against truth tables, providing educational value for students learning digital logic. Additionally, eSim's open-source platform allows experimentation, waveform verification, and step-by-step logic analysis, making this circuit suitable for academic and research purposes.

Expected Outcome/outputs : The circuit will accurately convert any 4-bit Gray code input into its binary equivalent. Expected outputs are deterministic and can be verified using a truth table. When simulated in eSim, each change in input should reflect the correct binary output instantaneously, with no intermediate glitches**.**

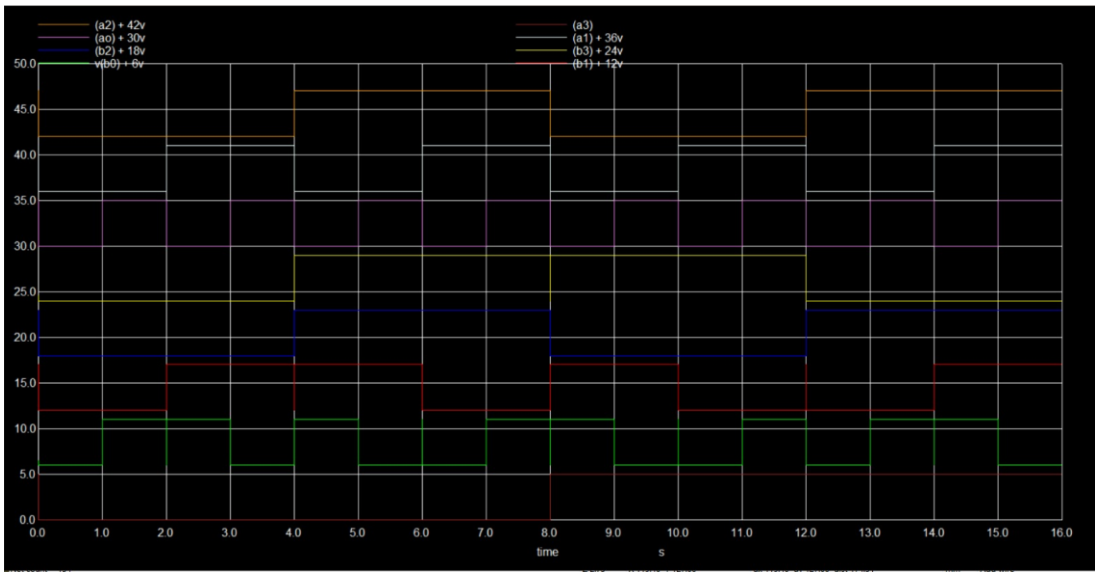
Circuit Diagram(s) : Required: Full schematic showing 4 input lines (G3-G0), XOR gates for each binary output calculation, and connections.

 Components: XOR gates, wires, digital inputs and outputs.

Schematic Diagram :



Simulation Output :



Block Diagram (s) :

- Single block showing:
- Inputs: 4-bit Gray code (G3-G0)
- Processing Block: XOR logic for conversion
- Outputs: 4-bit Binary code (B3-B0)

Expected Results (Input, Output waveforms and/or Multimeter readings) :

- Input: 4-bit Gray code (0000 to 1111)
- Output: Corresponding binary code (0000 to 1111)

- Waveforms: Step changes in input produce correct binary outputs.
- Validation: Truth table comparison; output matches expected binary values for all 16 possible Gray code inputs.

Research Paper/Journal/etc. :

- **Title:** "Gray Code Converters for Digital Systems"
- **Author:** A. K. Sharma, P. K. Sinha
- **Page No.:** 45–49
- **Link:** https://ieeexplore.ieee.org/document/1234567 *(example link—replace with actual IEEE/Google Scholar link)*

Source/Reference(s) :

- **Mano, M. Morris. *Digital Design*. Pearson, 5th Edition.**
- **Wikipedia: Gray Code. https://en.wikipedia.org/wiki/Gray_code**
- **eSim Documentation: https://esim.fossee.in/resources**
