Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

Name of the participant : SANTHOSH C

Affiliation / Institution : Department of Electronics Engineering (VLSI Design and Technology),Chennai Institute of Technology,Kanchepuram,Tamilnadu,India.

Title of the circuit : Design and Verification of an 8-Bit Carry Skip Adder Using eSim

Theory/Description :

Ripple Carry Adders (RCAs) suffer from large propagation delays due to linear carry dependency, which limits their applicability in low-power and high-speed digital systems. Post-2010 research has focused on optimizing Carry Skip Adders (CSKAs) using block-level propagate logic, multiplexed carry paths, and hybrid adder structures to reduce delay and power while maintaining moderate hardware complexity.

The objective of this project is to reproduce and migrate a post-2010 optimized 8-bit Carry Skip Adder architecture into the open-source eSim platform, verify its functional correctness using waveform analysis, and compare its performance behavior with a conventional Ripple Carry Adder.

An 8-bit Carry Skip Adder (CSKA) reduces carry propagation delay by dividing the adder into blocks and conditionally bypassing the carry across blocks when all propagate signals within a block are high.

Each bit generates a propagate signal Pi = Ai XOR Bi, indicating whether a carry can pass through that bit. For a block of bits, all propagate signals are AND-ed to form a block propagate signal. When this signal is high, the incoming carry skips the entire block through a multiplexer instead of rippling through each full adder, thereby reducing carry propagation delay.

Two 4-bit CSKA blocks

- Ripple logic inside each block
- Skip logic using AND gates and 2×1 MUX
- Final carry propagation through block-level bypass

Reason to Reproduce with eSim:

The circuit is reproduced using eSim because it supports mixed-signal simulation, allows easy verification of digital arithmetic circuits using open-source tools, and enables clear observation of input–output behavior without relying on proprietary simulators.

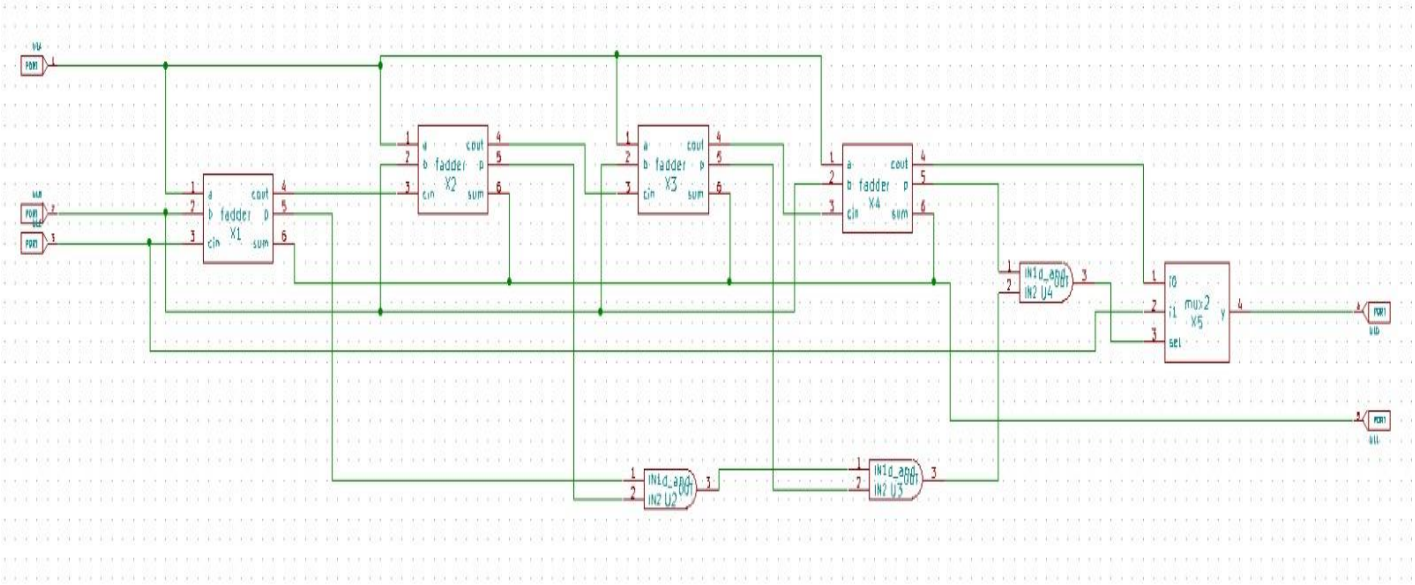
Expected Outcome/outputs :

- Correct 8-bit sum and carry for all input combinations
- Reduced effective carry propagation path when block propagate = 1
- Functional equivalence with RCA but improved carry behavior
- Successful reproduction of post-2010 CSKA architecture in eSim

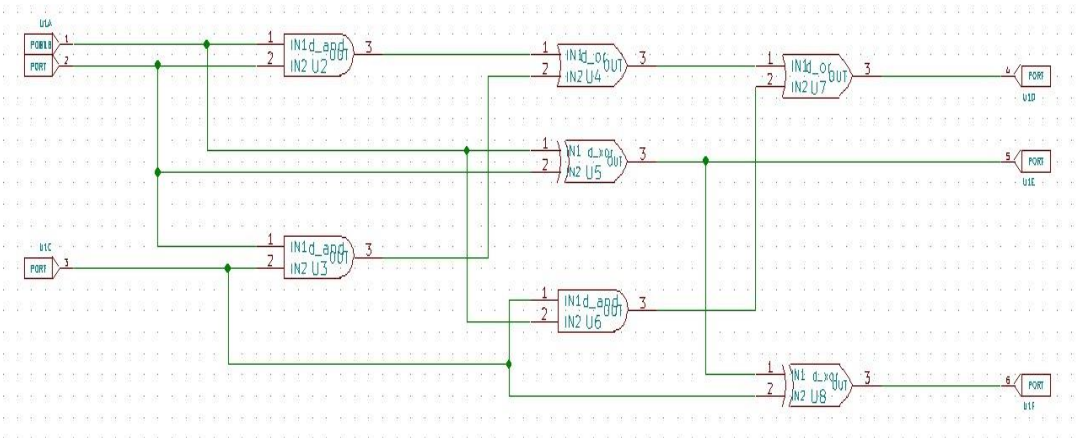
Circuit Diagram(s) :

This circuit converts analog pulse inputs into digital signals using ADC bridges, performs binary addition through cascaded full-adder blocks, and converts the resulting sum and carry outputs back to analog form using DAC bridges for simulation and verification in eSim.

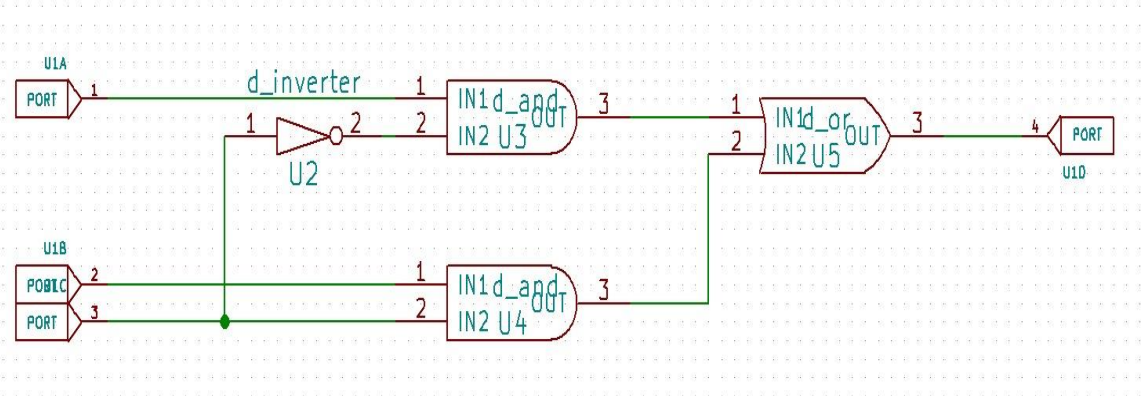
Schematic Diagram:



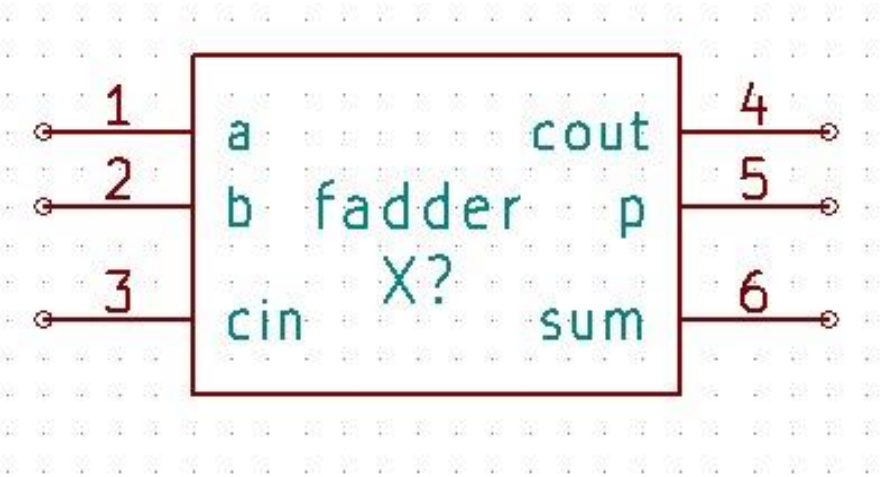
Img.1 Block Schematic Design



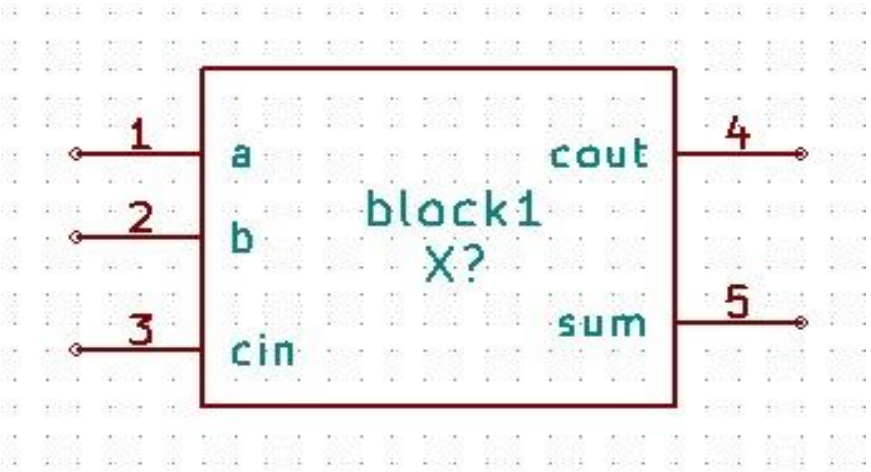
Img.2 Full Adder Schematic



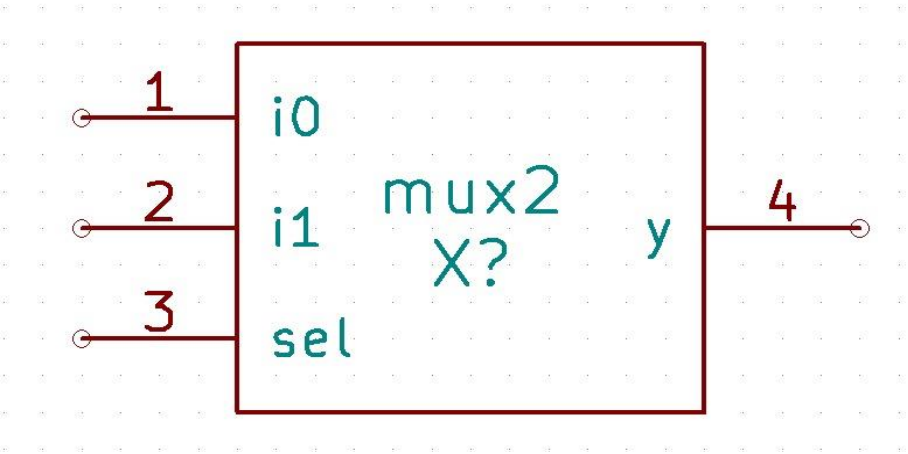
Img.3 Mux schematic Design



Img.4 Full Adder Subcircuit



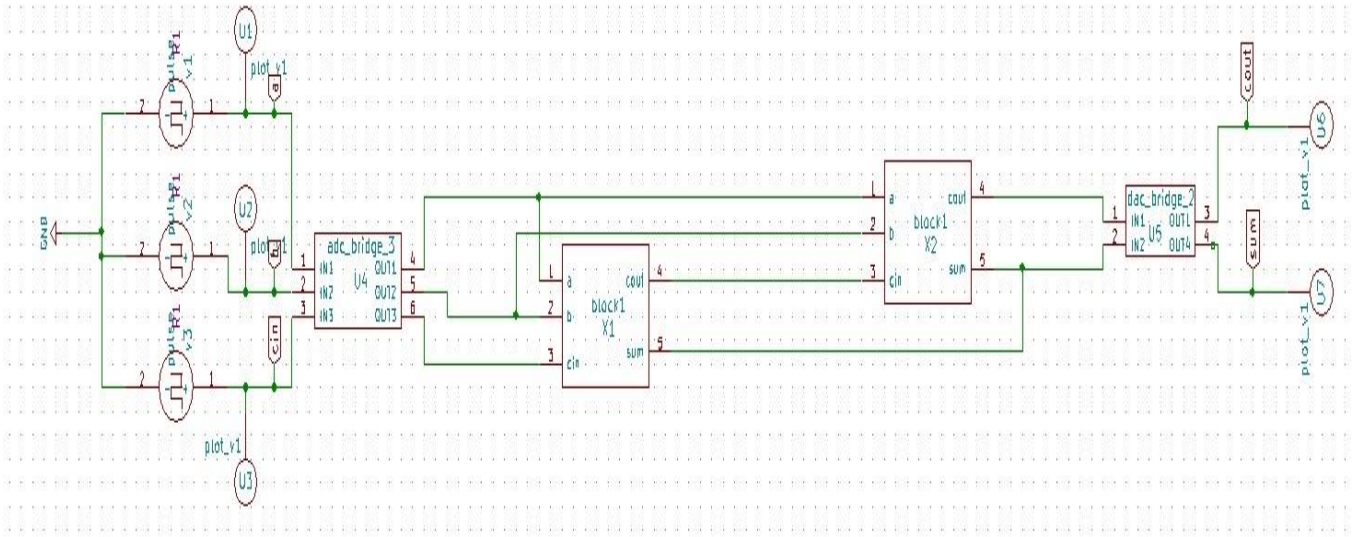
Img.5 Block Subcircuit



Img.6 Mux Subcircuit

Test Circuit :

The test circuit is designed to apply different combinations of input pulse signals to the adder circuit and verify its functionality through simulation by observing the corresponding sum and carry outputs, which are compared with the expected binary addition results to ensure correct operation.

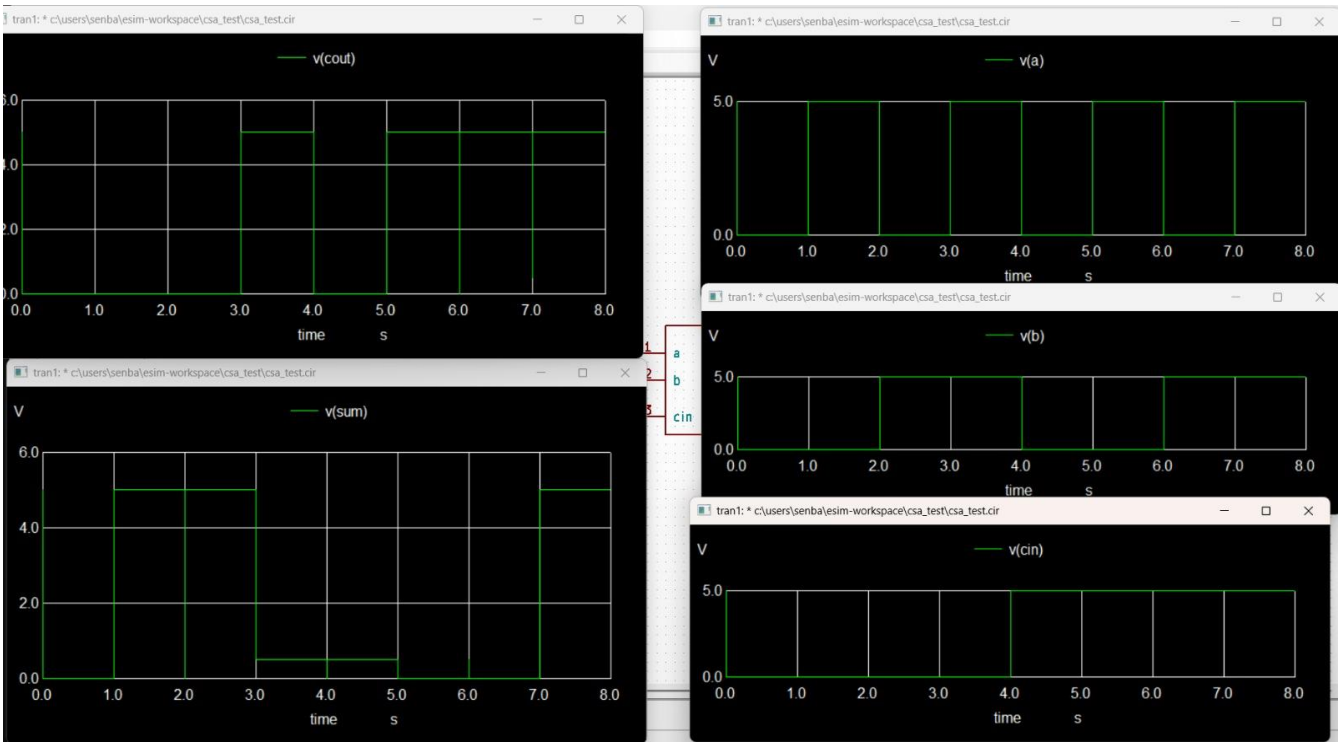


Img.7 Test Circuit

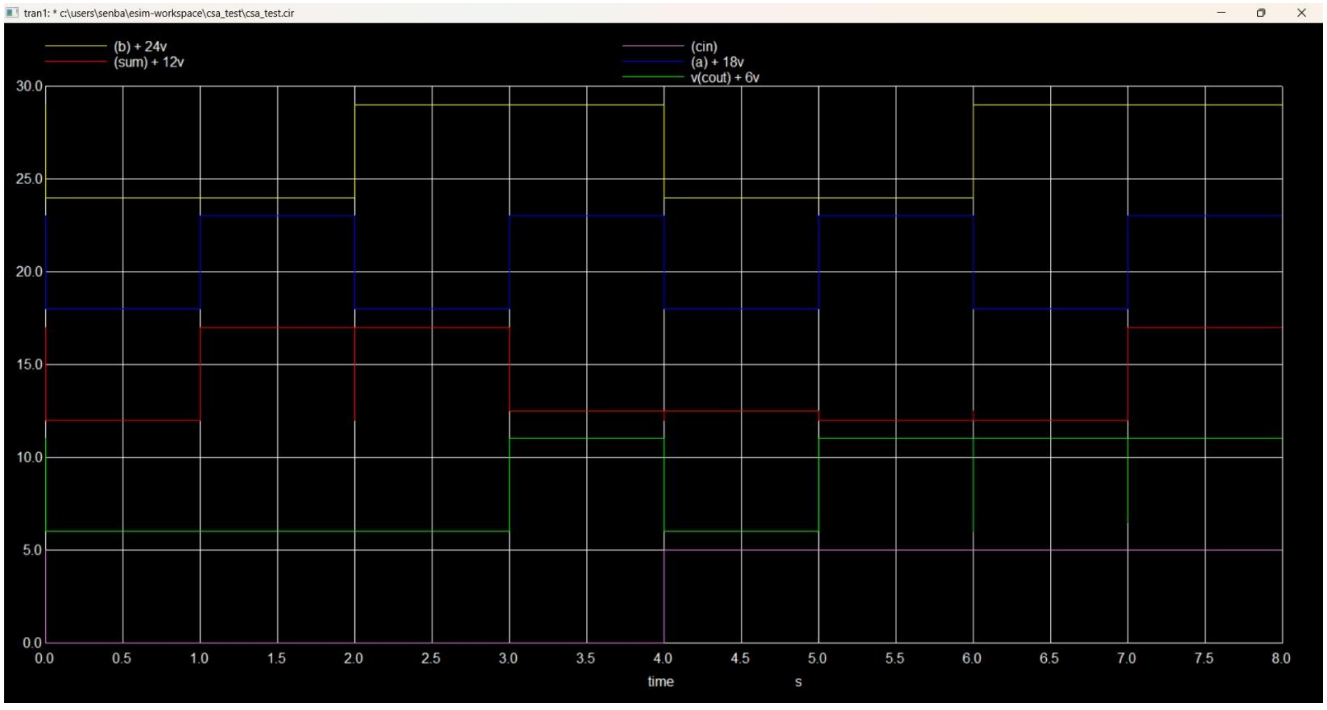
Expected Results :

The simulation outputs commonly show the relationship between the applied input signals and the resulting outputs , confirming that the circuit performs correct binary addition for all tested input combinations.

Simulation Output:



Img.8



Img.9

Truth Table :

a	b	cin	sum	cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	0	1	0
0	0	1	0	1
1	0	1	0	1
1	0	1	0	1
1	1	0	1	1

Research Paper/Journal/etc. :

Title: Performance Analysis of High-Speed Carry Skip Adders
Authors: M. Alioto, G. Palumbo
Year: 2011
Source: IEEE Transactions on Very Large Scale Integration (VLSI) Systems
Link: https://ieeexplore.ieee.org

Relevance:
This paper analyzes the delay, power, and area characteristics of carry skip adders and demonstrates their suitability for low-power and moderate-speed arithmetic applications, supporting the design choices used in this 8-bit CSKA implementation.