

Design and Implementation of an 8x1 Multiplexer Using 2x1 Multiplexer Modules

SUBIKEESH M

*Dept of Electronics Engineering
(VLSI Design and Technology)
Rajalakshmi Institute of Technology*

Dr. MAHESWARI RAJA

*Principal
Rajalakshmi Institute of Technology*

Abstract

This project focuses on the design and optimization of an 8×1 multiplexer using 2×1 multiplexer building blocks to achieve high speed, low power consumption, and efficient hardware utilization. A hierarchical design approach is employed to reduce propagation delay and logic complexity. The circuit is simulated and verified using eSim to ensure correct functionality and reliable performance. The modular structure of the design allows easy scalability and makes it suitable for real-time digital systems, embedded applications, and VLSI implementations.

Keywords: 8×1 Multiplexer, 2×1 Multiplexer, Digital Logic Design, Combinational Circuits, Hierarchical Design, Signal Selection, Hardware Optimization

INTRODUCTION

Multiplexing is one of the most fundamental operations in digital systems, widely used in applications such as data routing, communication systems, processor architectures, and embedded systems. The efficiency of a multiplexer circuit directly influences the overall performance of digital systems, as it affects speed, power consumption, and hardware utilization. Conventional multiplexer designs, while functional, often suffer from increased propagation delay and higher logic complexity when implemented using larger input sizes. This project focuses on the design and optimization of an 8×1 multiplexer circuit using 2×1 multiplexers, aiming to achieve high speed, reduced delay, and efficient hardware usage. By adopting a hierarchical design approach, the work provides a reliable solution for real-time digital and low-power VLSI applications.

Purpose of 8×1 Multiplexer

1. To select and route one of multiple input signals to a single output efficiently
2. To minimize propagation delay and ensure high-speed data selection
3. To reduce hardware complexity through hierarchical design using 2×1 multiplexers
4. To achieve low power consumption suitable for VLSI applications
5. To support real-time digital systems, communication, and embedded applications

WORKING PRINCIPLE

1. **Input Selection:** Eight data inputs are provided along with three select lines.
2. **First-Level Selection:** Pairs of inputs are selected using 2×1 multiplexers based on the least significant select line.
3. **Intermediate Selection:** The outputs from the first stage are further selected using the next select line.
4. **Final Selection:** A single 2×1 multiplexer controlled by the most significant select line produces the final output.
5. **Optimization:** Hierarchical design minimizes propagation delay, power consumption, and hardware complexity.

CIRCUIT DIAGRAM

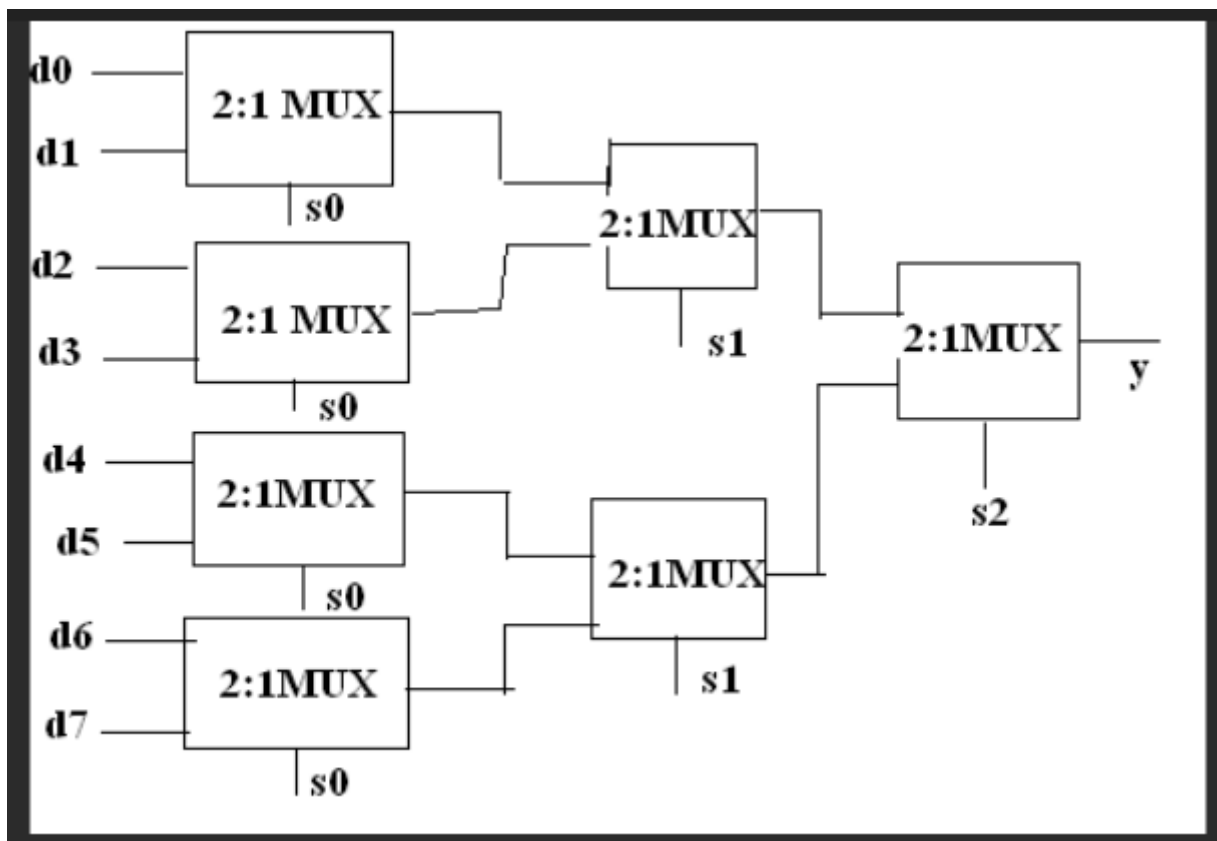


Fig 1: 8×1 Multiplexer

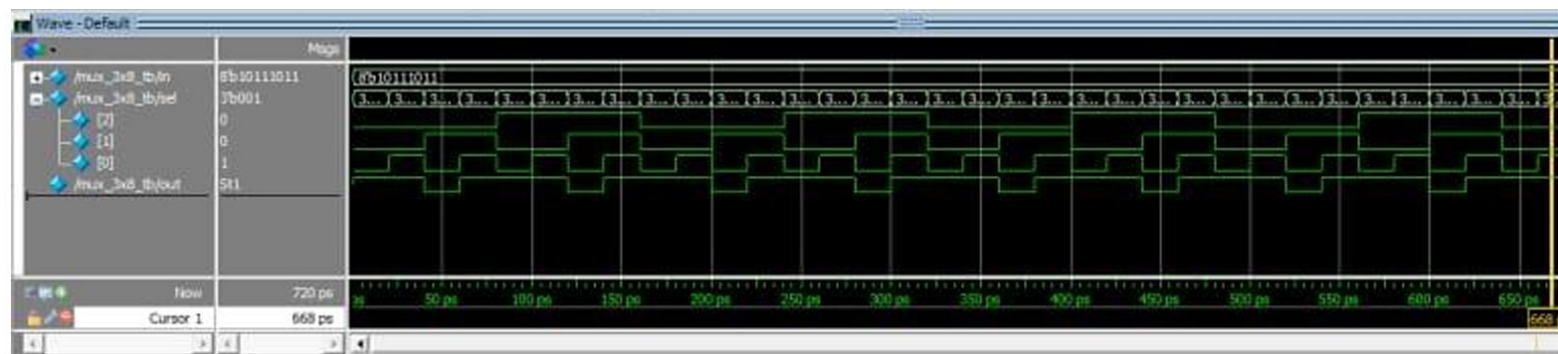


Fig 2: Output

PROPOSED SYSTEM

The proposed system focuses on designing an optimized **8×1 multiplexer** using **2×1 multiplexer modules** to achieve high speed and efficient operation. The design follows a hierarchical structure where input signals are selected in multiple stages using select lines, ensuring accurate and fast data routing to the output. This approach minimizes propagation delay, power consumption, and hardware complexity. The optimized multiplexer design is suitable for real-time digital systems, embedded applications, and VLSI circuit implementations.

ESIM CIRCUIT

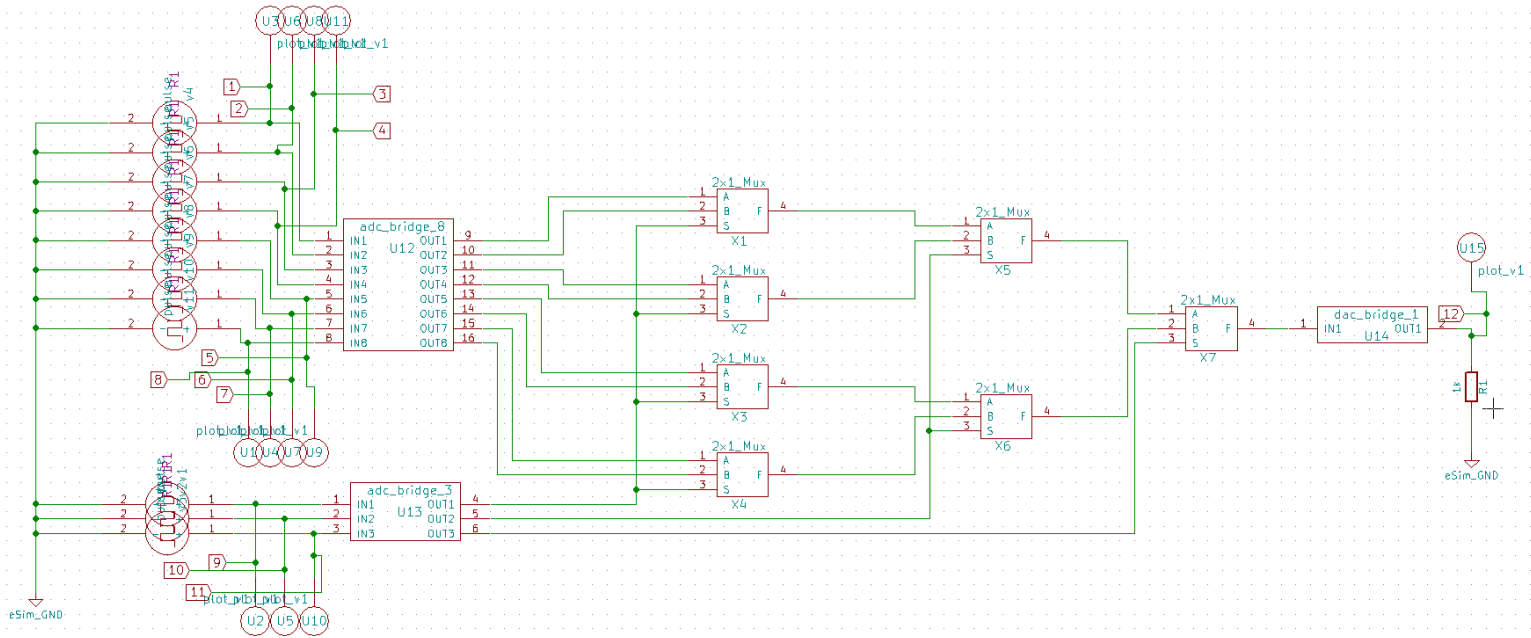
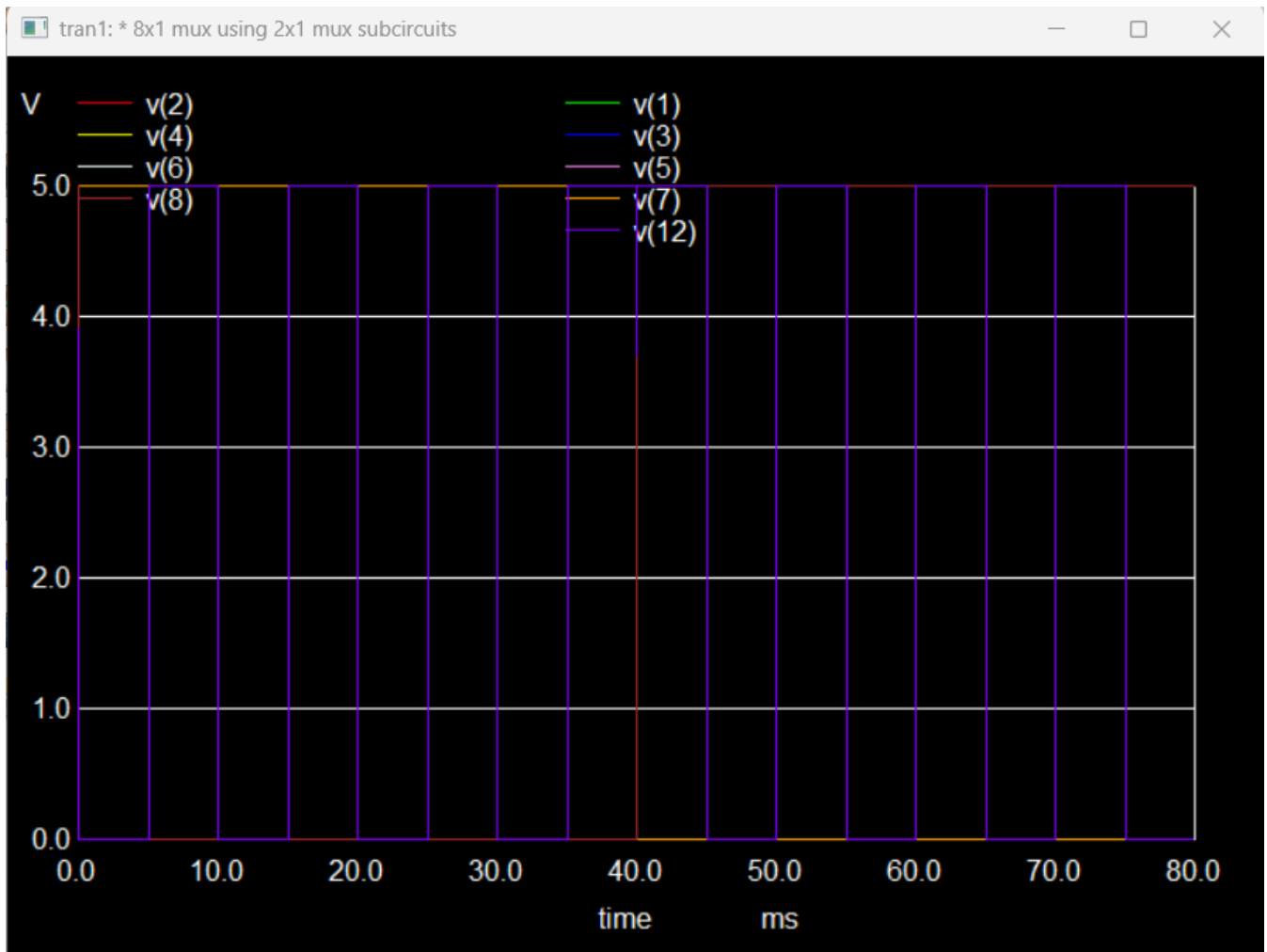
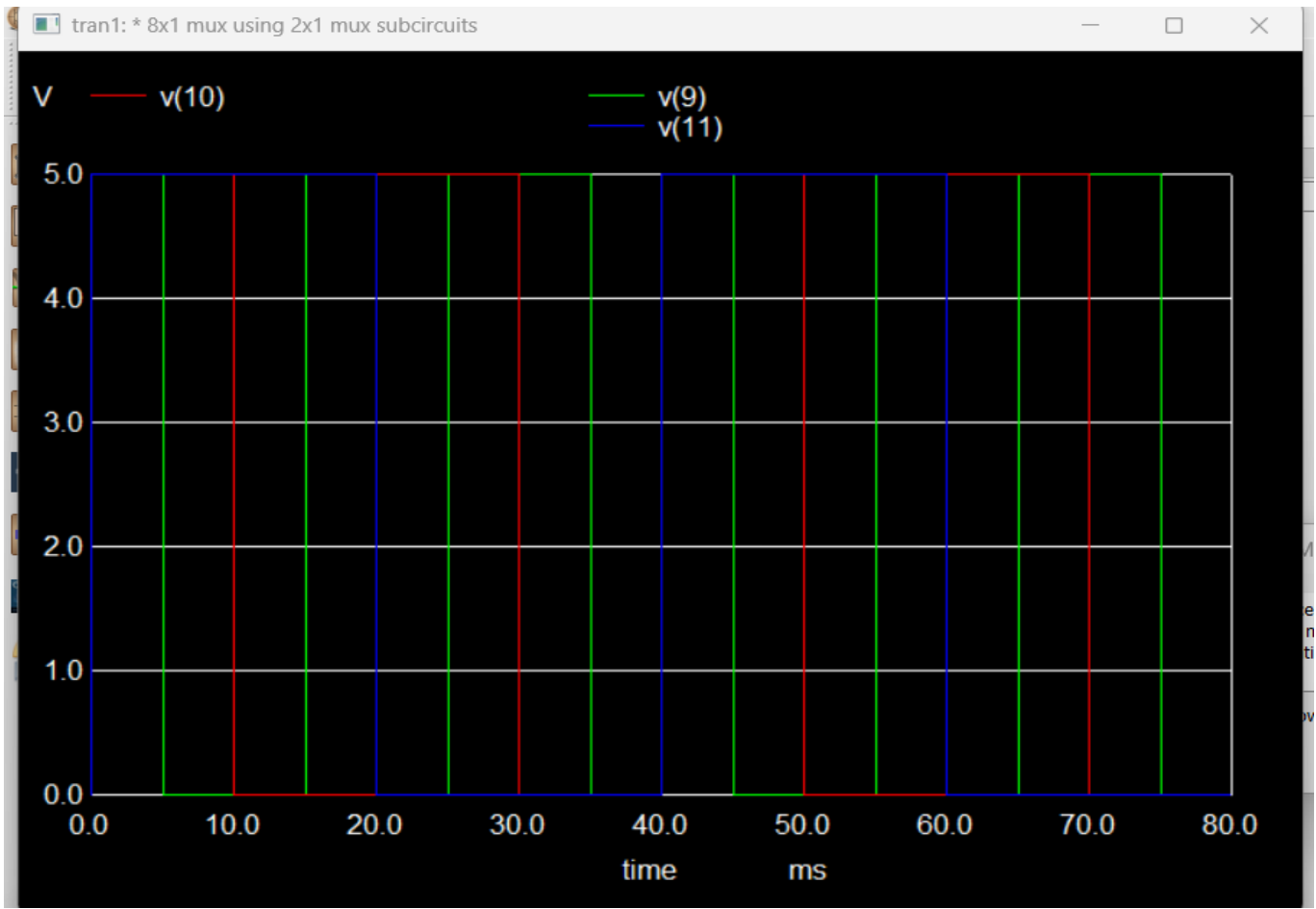


Fig 3: eSim Circuit Diagram

WAVEFORM OF 8*1 MULTIPLEXER





Advantages of 8×1 Multiplexer

1. High-speed data selection
2. Low power consumption
3. Reduced hardware complexity using 2×1 MUX building blocks
4. Accurate and reliable signal routing
5. Suitable for real-time digital and embedded applications

Disadvantages of 8×1 Multiplexer

1. Increased number of components compared to a single 2×1 multiplexer
2. Propagation delay due to multiple selection stages
3. Higher hardware usage when implemented using discrete logic blocks
4. Complexity increases when extending to higher-order multiplexers

1.

Applications of 8×1 Multiplexer

1. Data selection and routing in digital systems
2. Communication systems and data transmission
3. Embedded systems
4. Processor and microcontroller architectures
5. VLSI and ASIC design
6. Bus switching and control logic
7. Real-time digital and control systems

Conclusion:

The **8×1 multiplexer** provides an efficient and high-speed solution for data selection in digital systems. By using a hierarchical design with 2×1 multiplexers, the circuit reduces propagation delay, power consumption, and hardware complexity. This makes it suitable for applications in communication systems, embedded platforms, and VLSI circuits where fast and reliable signal routing is essential. Overall, the optimized 8×1 multiplexer improves system performance while maintaining energy efficiency and scalability for higher-order multiplexer designs.

REFERENCES

1. <https://youtu.be/uoBZZ53Okvo?si=cHKWML2Soo8KmG65>
2. [Designing an 8x1 Multiplexer Using 2x1 Multiplexers in Verilog | by Mahnoor Zia | Medium](#)
3. [Design and implement the 8x1 MULTIPLEXER with 2x1 MULTIPLEXERs program using Verilog HDL - IC Applications and ECAD Lab | vikramlearning.com](#)