

# Dual Dynamic node Hybrid FlipFlop

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## Abstract

This work describes the operation of a dual dynamic node hybrid flip-flop (DDFF) architecture, in which two internal nodes, X1 and X2, operate as pseudo-dynamic and dynamic nodes, respectively. Both nodes are weakly retained using inverter-based keepers, offering improved robustness compared to conventional XCFF structures. Unlike conditional shutoff techniques, the proposed DDFF employs an unconditional shutoff mechanism at the front end, simplifying control and reducing contention.

The flip-flop operates in two distinct phases: evaluation and precharge. During the evaluation phase ( $CLK = 1$ ), data evaluation and potential latching occur when the clock and its complement overlap. If the input has high priority during this overlap, node X1 discharges, triggering a change in inverter states that propagates to the output through controlled discharge paths. In this phase, node X2 is held high by a PMOS device, preventing unintended transitions. During the precharge phase ( $CLK = 0$ ), node X1 is precharged to logic high, while node X2 retains its stored charge dynamically without direct driving. Output stability is ensured through static inverter stages.

Overall, the DDFF architecture effectively combines dynamic and pseudo-dynamic storage elements to achieve reliable high-speed operation with reduced power dissipation and improved noise immunity, making it suitable for low-power and high-performance VLSI applications.

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## I. INTRODUCTION

Flip-flops are fundamental sequential elements in digital integrated circuits, extensively used in high-speed processors, communication systems, and low-power VLSI designs. With aggressive CMOS technology scaling, conventional static and dynamic flip-flop architectures face major challenges such as increased leakage power, reduced noise margins, clock overlap sensitivity, and excessive power dissipation due to unnecessary switching activity.

Dynamic and hybrid flip-flop designs have been proposed to improve speed and reduce transistor count; however, they often suffer from charge leakage, poor data retention, and vulnerability to noise, especially at low supply voltages. Conditional shutoff mechanisms, commonly used to reduce short-circuit current, add extra control circuitry and increase design complexity.

To address these limitations, the **Dual Dynamic Node Hybrid Flip-Flop (DDFF)** architecture introduces a combination of pseudo-dynamic and dynamic storage nodes with an unconditional shutoff mechanism. This design improves robustness, reduces contention, and maintains high-speed operation while achieving lower power consumption compared to traditional flip-flop structures such as the XCFF.

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## Problem Statement

With continuous scaling of CMOS technology, conventional flip-flop architectures face critical challenges such as increased power dissipation, reduced noise margins, charge leakage in dynamic nodes, and unreliable data retention at low supply voltages. High-speed hybrid and dynamic flip-flops often rely on conditional shutoff mechanisms to minimize contention and short-circuit currents; however, these techniques introduce additional control circuitry, increasing design complexity and area overhead. Furthermore, fully dynamic internal nodes are highly susceptible to leakage and coupling noise, which degrades robustness during extended evaluation periods. As a result, existing flip-flop designs struggle to achieve an optimal balance between speed, power efficiency, noise immunity, and circuit simplicity. Therefore, there is a strong need for a flip-flop architecture that ensures reliable operation under deep-submicron conditions while reducing power consumption and complexity, without compromising performance.

## Working Principle

The DDFF operates based on two clock-controlled phases: **evaluation** and **precharge**, utilizing two internal nodes—**X1** (pseudo-dynamic) and **X2** (dynamic).

### 3.1 Evaluation Phase (CLK = 1)

When the clock signal is high, the flip-flop enters the evaluation phase. During this phase, data evaluation and latching occur when the clock and its complement briefly overlap. If the input data has high priority during this overlap period, node **X1** discharges through a conduction path formed by NMOS transistors. This discharge causes a change in the state of the inverter pair connected to X1, resulting in node **X1B** transitioning to logic high.

As a consequence, the output node **QB** begins to discharge through an NMOS transistor, propagating the evaluated data to the output stage. Inverters connected to X1 maintain the discharged state for the remainder of the evaluation phase, preventing unintended recharging. During this entire phase, node **X2** is held at logic high by a PMOS transistor, ensuring output stability and avoiding false switching.

### 3.2 Precharge Phase (CLK = 0)

When the clock transitions from high to low, the circuit enters the precharge phase. In this phase, node **X1** is precharged to logic high through a PMOS transistor, resetting the evaluation path and restoring the initial conditions of the inverter stages.

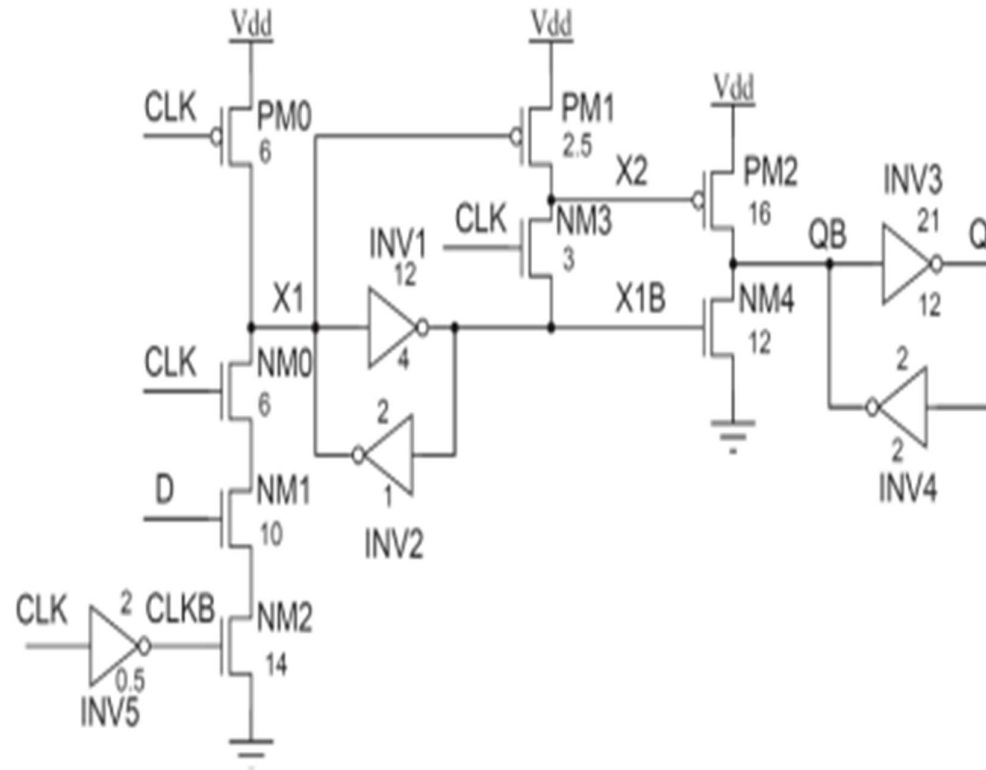
Simultaneously, node **X2** retains its stored charge dynamically and is not actively driven by any transistor. The output is maintained by static inverter stages, ensuring data stability even during dynamic charge retention. This phase prepares the flip-flop for the next evaluation cycle.

### 3.3 Data Retention and Output Operation

When **CLK = 1** and **D = 0**, node **X1** remains at logic high, while node **X2** is discharged through an NMOS transistor. This causes the output node **Q** to charge to logic high through a PMOS transistor, with the corresponding NMOS device remaining off. Weak inverter-based keepers associated with nodes X1 and X2 enhance charge retention and noise immunity without significantly impacting performance.

## CIRCUIT DIAGRAM

NOT FORMING OUT.



## eSim Circuit

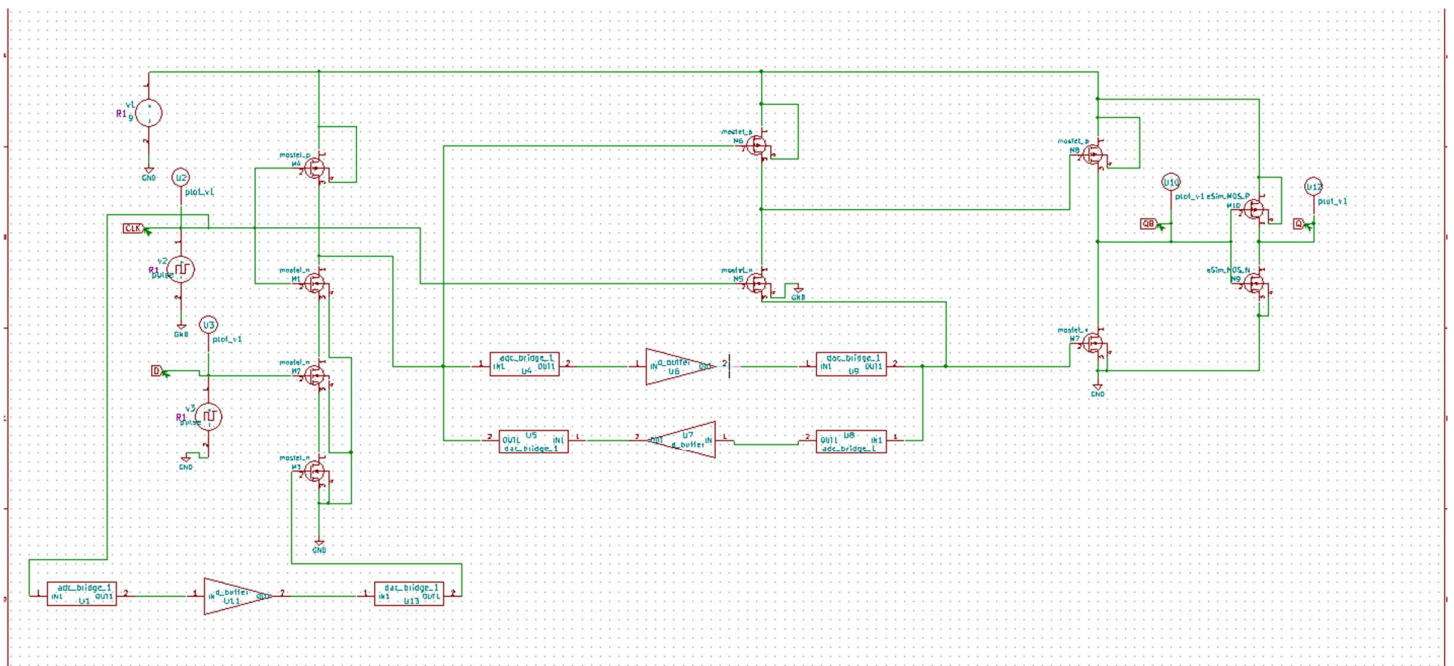
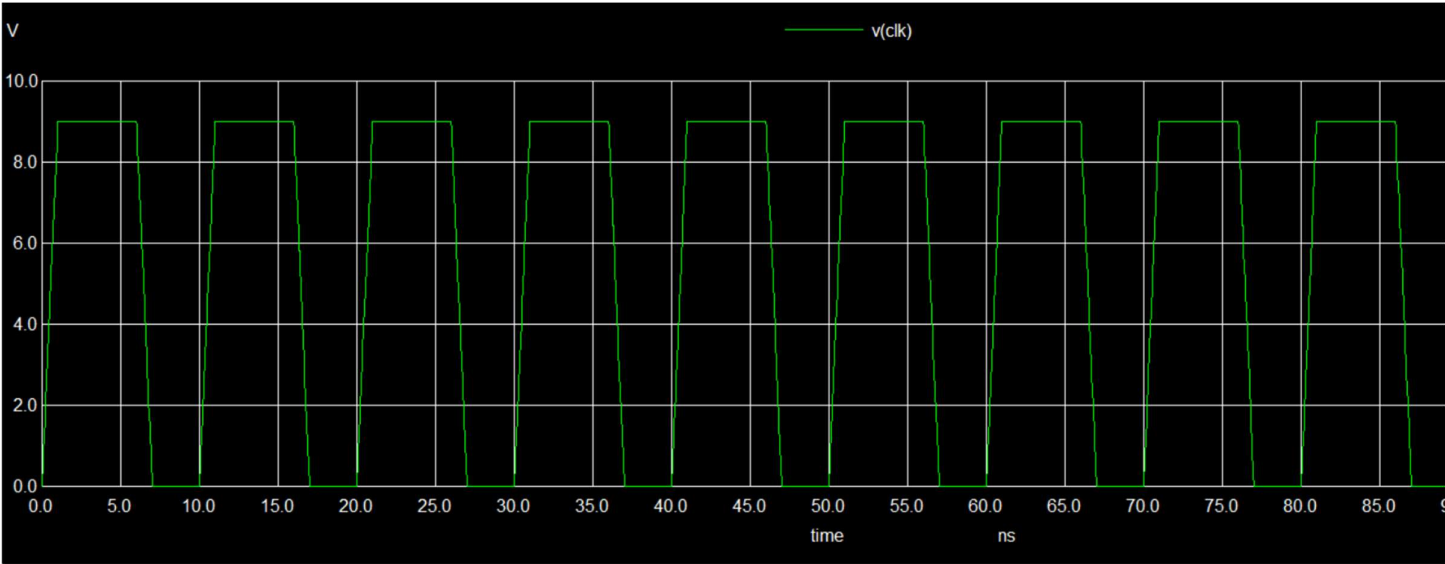
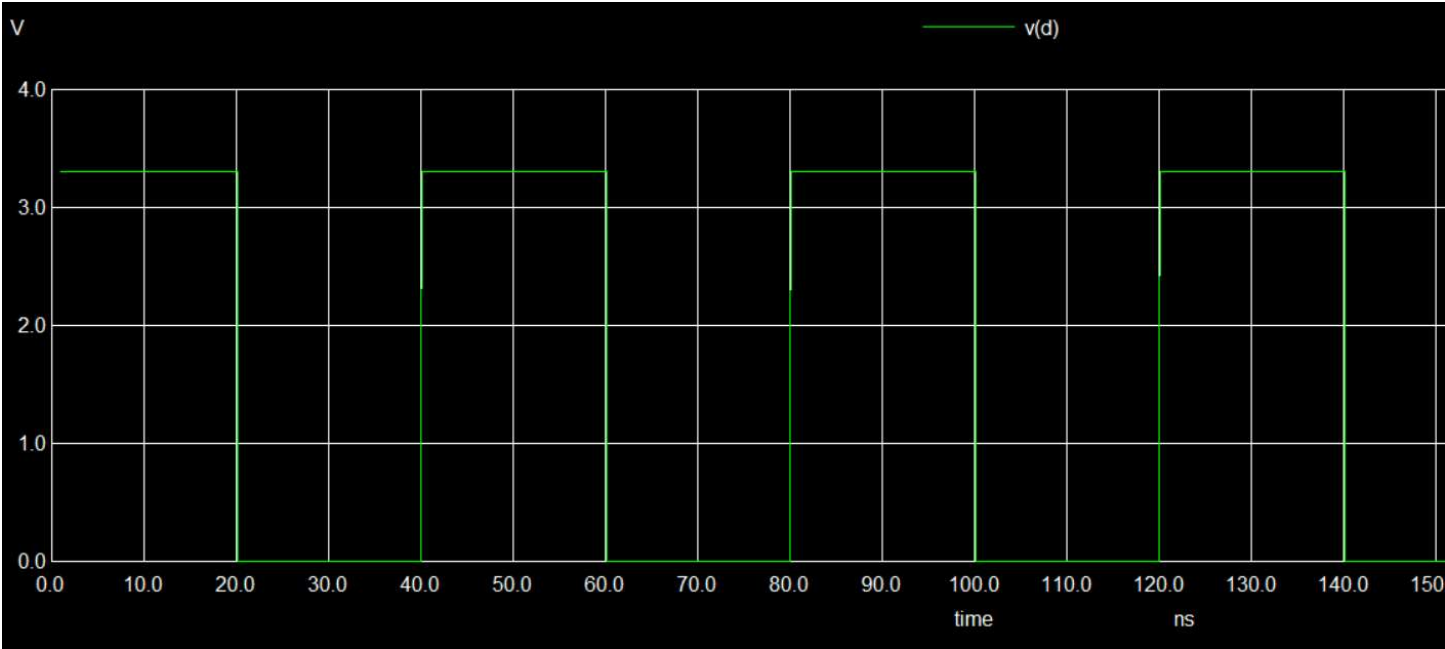


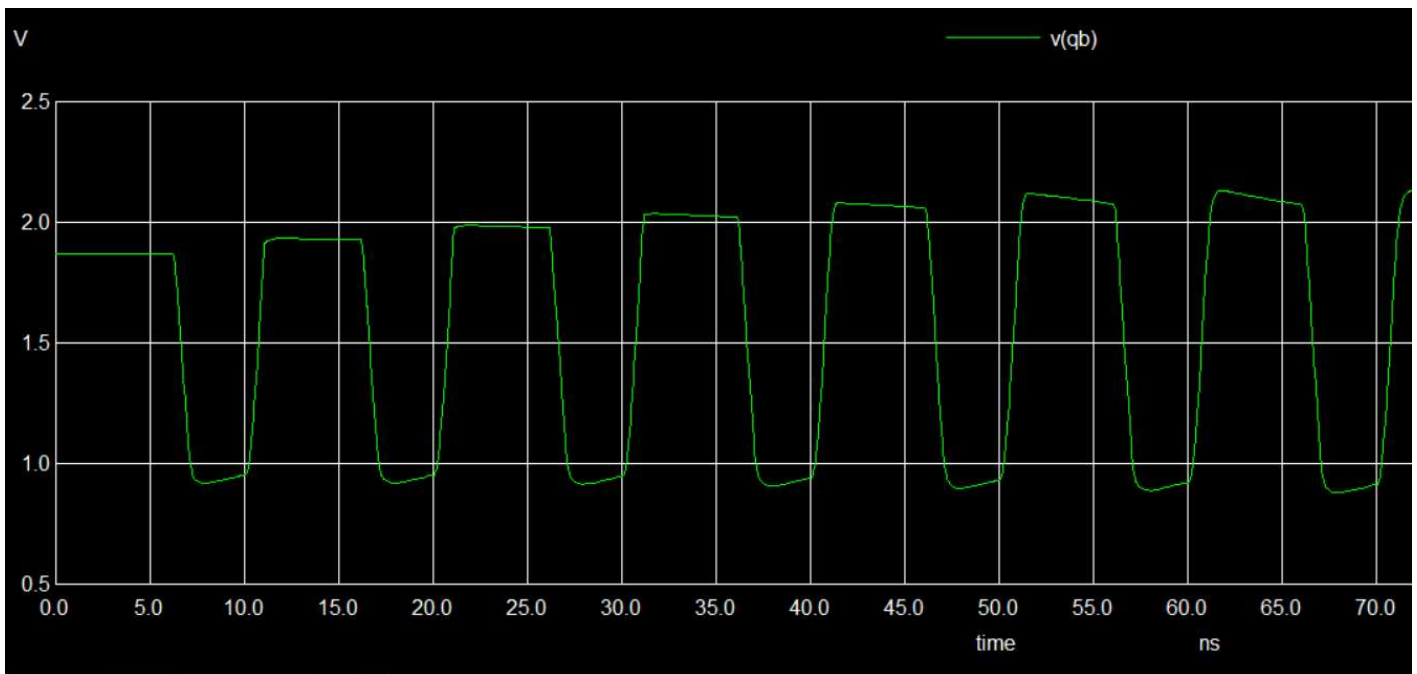
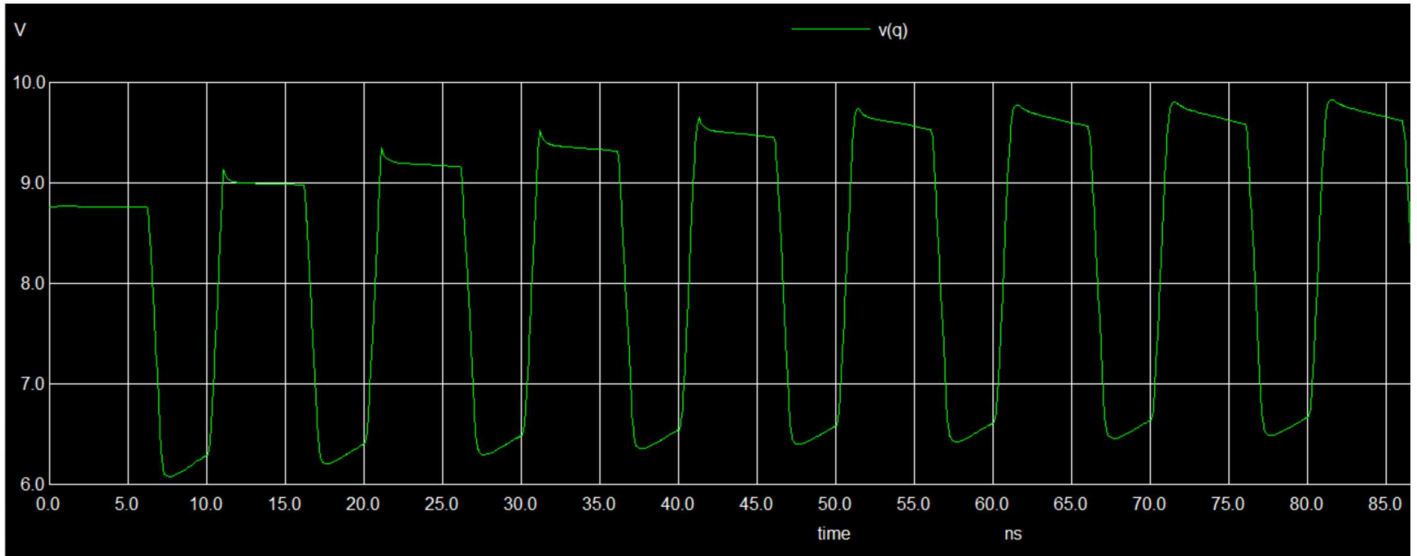
Fig: Circuit Diagram of Dual dynamic node hybrid Flipflop

**INPUT WAVEFORM**



**Fig: Input waveforms of Dual dynamic node hybrid flipflop**

**OUTPUT WAVEFORM:**



## CONCLUSION:

The Dual Dynamic Node Hybrid Flip-Flop (DDFF) architecture effectively addresses the limitations of conventional dynamic and hybrid flip-flops by combining pseudo-dynamic and dynamic storage nodes with an unconditional shutoff mechanism. The use of weak inverter-based keepers enhances charge retention and noise immunity, while eliminating the need for complex conditional shutoff circuitry. The two-phase operation—evaluation and precharge—ensures reliable data capture and stable output behavior across clock transitions. As a result, the DDFF achieves improved robustness, reduced power dissipation, and simplified circuit design without sacrificing high-speed performance. These characteristics make the proposed flip-flop well suited for low-power and high-performance VLSI applications in deep-submicron CMOS technologies.

## REFERENCE:

K. Absel, L. Manuel, and R. K. Kavitha, "Low-Power Dual Dynamic Node Pulsed Hybrid Flip-Flop Featuring Efficient Embedded Logic," *IEEE Trans. VLSI Syst.*, vol. 21, no. 9, pp. 1693–1704, Sep. 2013, doi: 10.1109/TVLSI.2012.2213280

