Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

Name of the participant : S S JHOTHEESHWAR

Affiliation / Institution : Electronics Engineering - VLSI Design and Technology, Chennai Institute of Technology, Chennai, Tamilnadu, India

Title of the circuit : Implementation of a Multi-Mode Universal Flip-Flop Using a Single Storage Element

Theory/Description :

A universal flip-flop is a configurable sequential digital circuit that can perform the functions of D, T, JK, and SR flip-flops using a single storage element. Instead of implementing each flip-flop separately, the universal flip-flop employs mode-select control signals to choose the required operation, thereby reducing hardware redundancy and improving area efficiency. The design is based on the concept of generating a unified next-state value through combinational logic corresponding to the selected flip-flop mode.

The circuit uses a single edge-triggered D flip-flop as the storage element, with multiplexers, XOR gates, and inverters forming the next-state logic. Based on the selected mode, the appropriate next-state value is applied to the D input of the flip-flop, and the output state updates on the active clock edge. Feedback from the output enables toggle and hold operations, while an asynchronous reset initializes the circuit to a known state. This architecture provides an efficient and flexible solution for implementing reconfigurable sequential logic in digital systems.

Reason to reproduce with eSim :

The universal flip-flop is suitable for eSim simulation due to its open-source accessibility and ease of digital logic verification. eSim allows clear observation of mode-select behavior and efficient validation of the circuit's functionality through waveform analysis.

Expected Outcome/outputs :

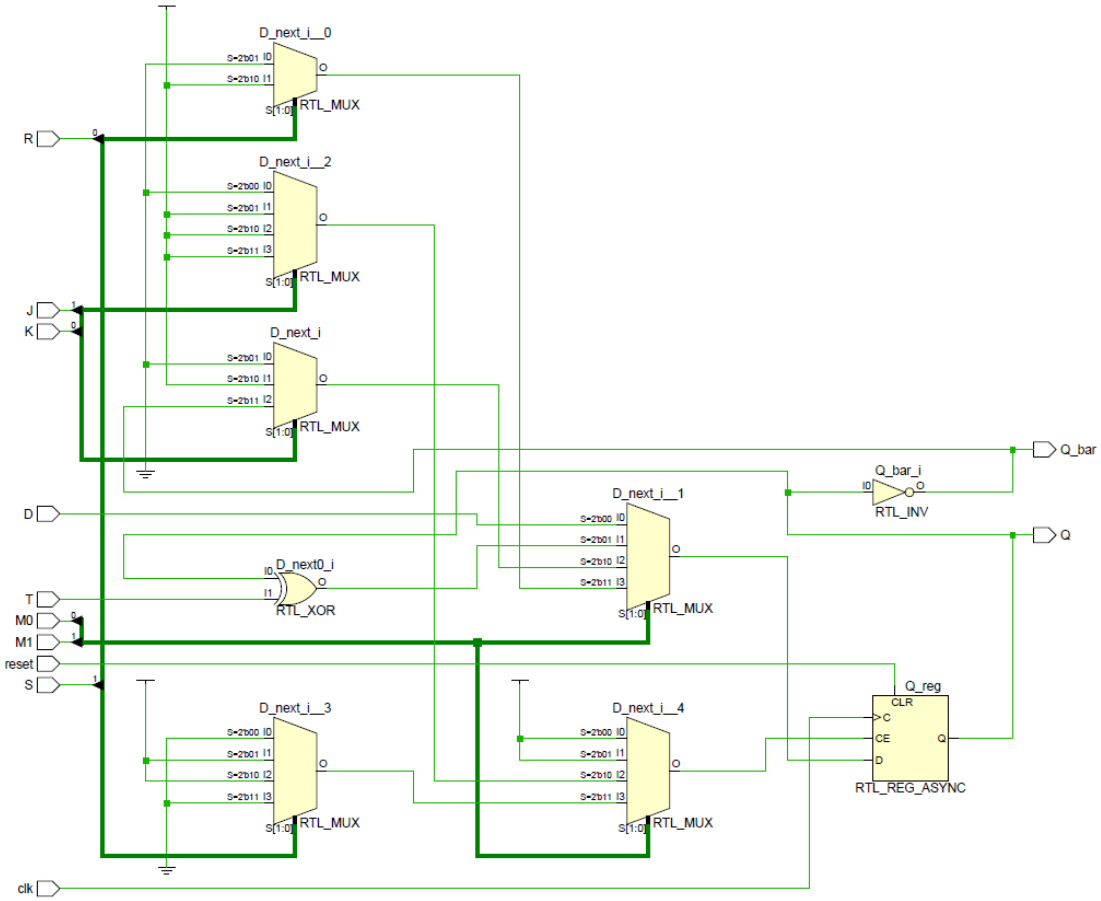
When simulated or implemented, the universal flip-flop is expected to operate according to the selected mode control signals. For mode 00, the circuit behaves as a D flip-flop, where the output follows the D input on the active clock edge. For mode 01, it functions as a T flip-flop, toggling the output when T is high. For mode 10, it behaves as a JK flip-flop, performing set, reset, hold, or toggle

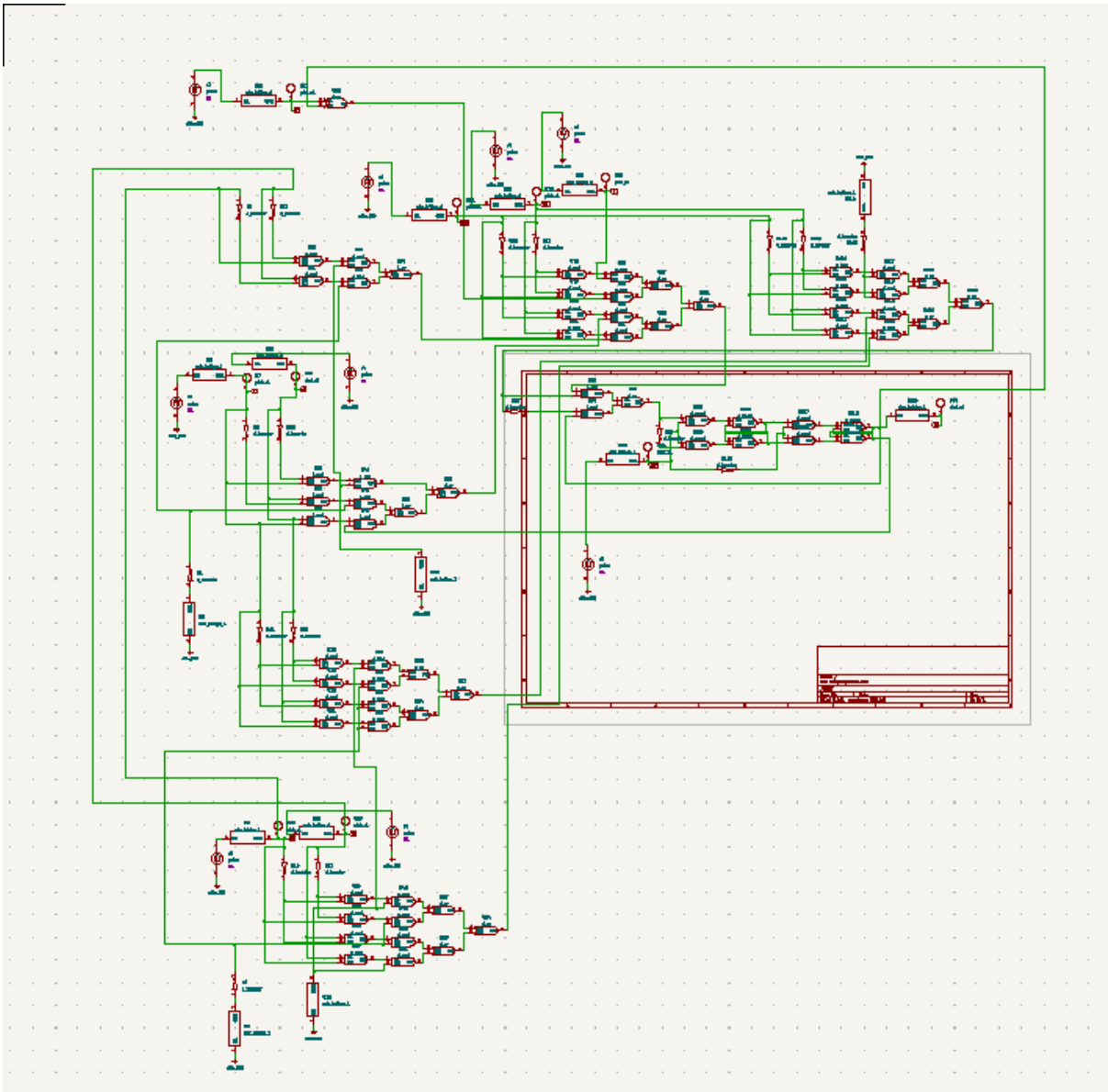
operations based on J and K inputs. For mode 11, it operates as an SR flip-flop, setting or resetting the output according to S and R inputs.

The correct operation is validated by observing simulation waveforms, ensuring that the mode-select multiplexing routes the appropriate next-state logic to the flip-flop and that the output Q updates only on clock edges. Matching the observed behaviour with the theoretical truth tables of each flip-flop confirms proper functionality of the circuit.

Circuit Diagram(s) :

- The circuit implements a universal flip-flop that operates as D, T, JK, or SR flip-flop based on mode-select inputs M1 and M0.
- Multiplexers (RTL_MUX) are used to select the appropriate next-state logic for each mode, routing the selected output to the D input.
- XOR and inverter logic support toggle operation and generate the complementary output.
- A single D flip-flop with Clock Enable (CE) is used as the storage element, ensuring controlled state updates on the clock edge.



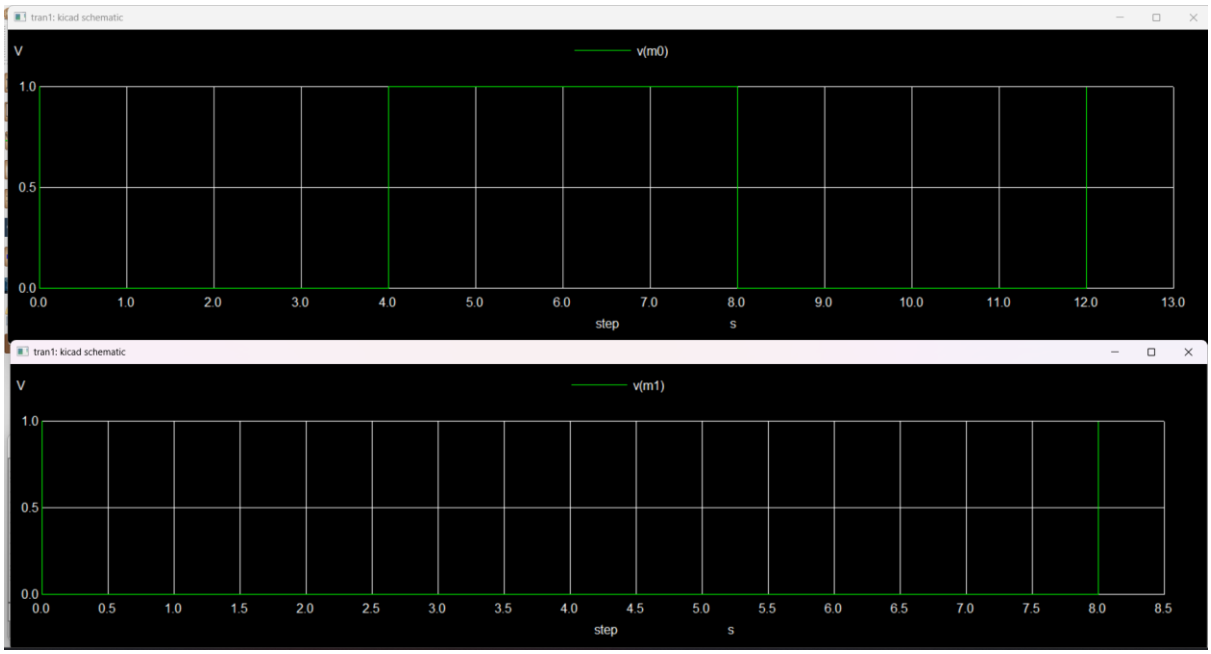


Expected Results (Input, Output waveforms and/or Multimeter readings) :

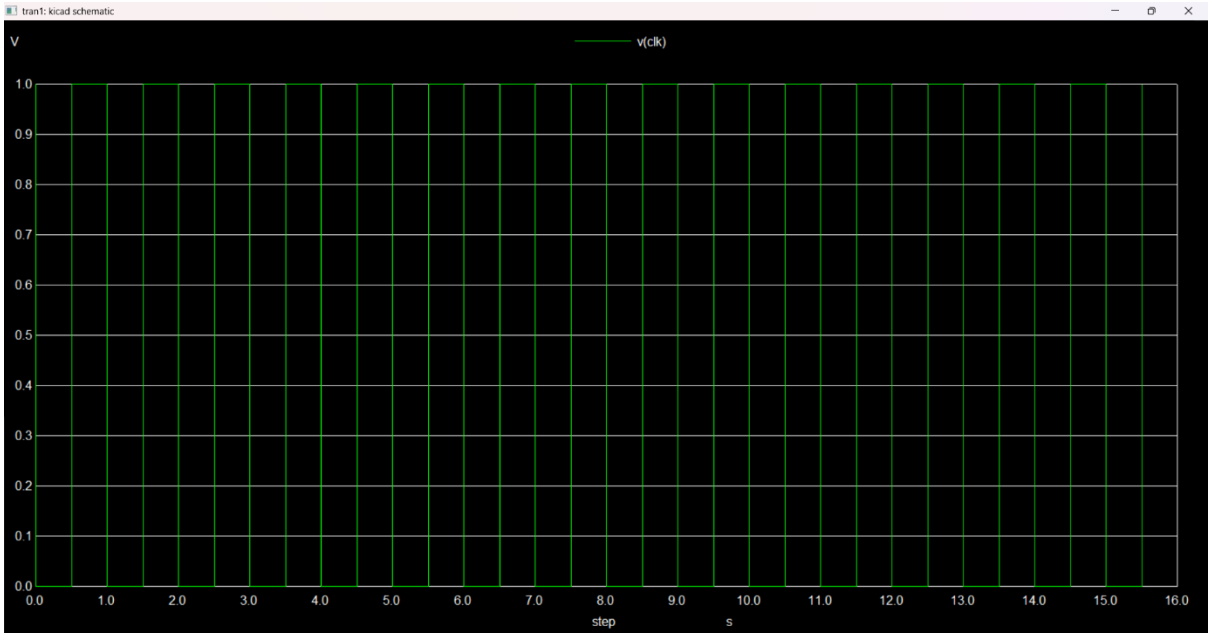
The circuit is driven by a clock, reset, mode-select signals (M1, M0), and data/control inputs (D, T, J, K, S, R). The clock is a periodic square wave, and the reset initializes the output to logic 0.

The output Q updates only on the active clock edge according to the selected mode (00–D, 01–T, 10–JK, 11–SR), while $\bar{Q}$ remains the complement of Q. Correct operation is verified by observing clock-aligned output transitions in the simulation waveform.

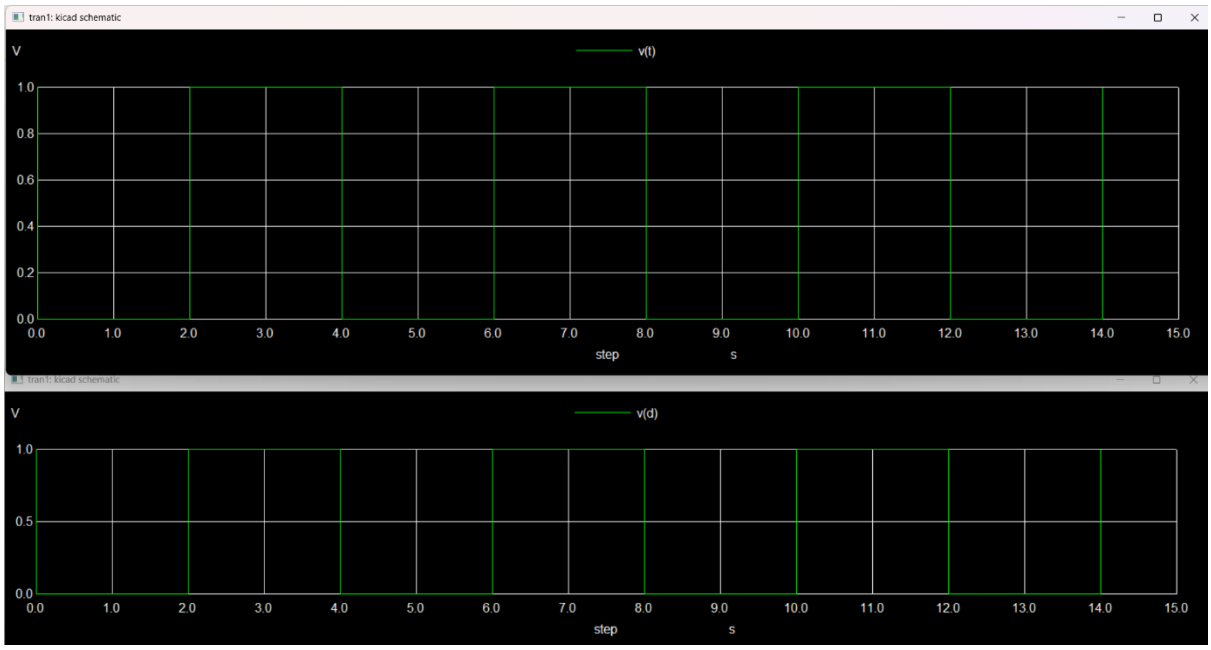
M0 & M1


tran1: kicad schematic
V
v(m0)
1.0
0.5
0.0
0.0 1.0 2.0 3.0 4.0 5.0 6.0 7.0 8.0 9.0 10.0 11.0 12.0 13.0
step
s
tran1: kicad schematic
V
v(m1)
1.0
0.5
0.0
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 5.0 5.5 6.0 6.5 7.0 7.5 8.0 8.5
step
s

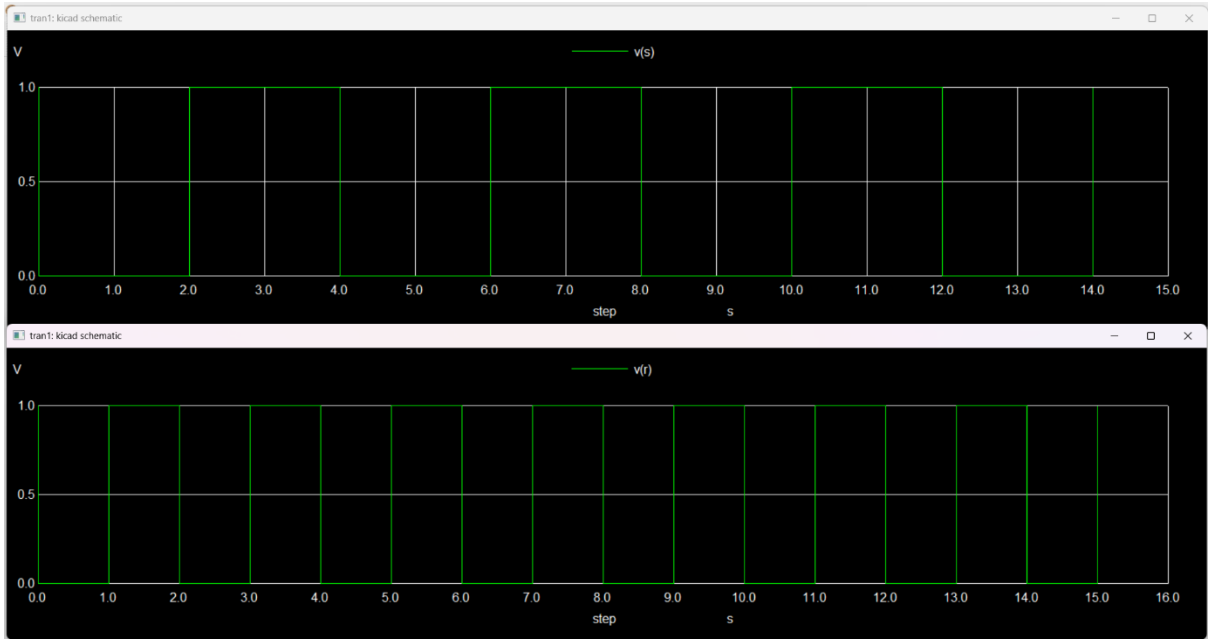
CLK


tran1: kicad schematic
V
v(clk)
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0.0 1.0 2.0 3.0 4.0 5.0 6.0 7.0 8.0 9.0 10.0 11.0 12.0 13.0 14.0 15.0 16.0
step
s

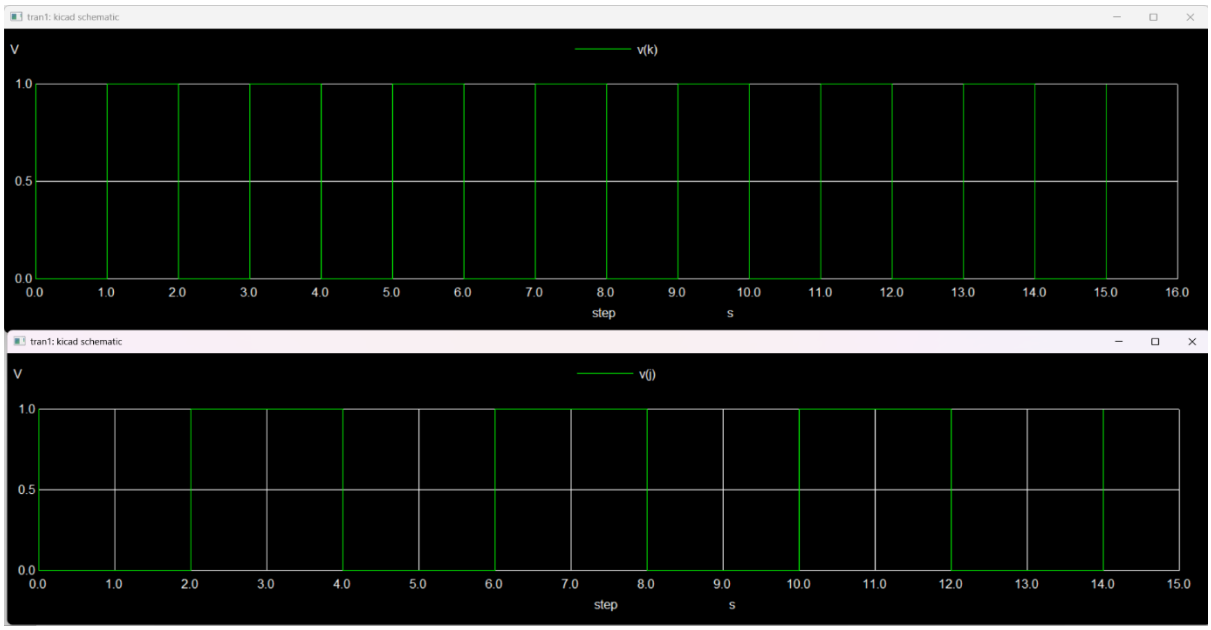
CONTROL INPUTS D & T



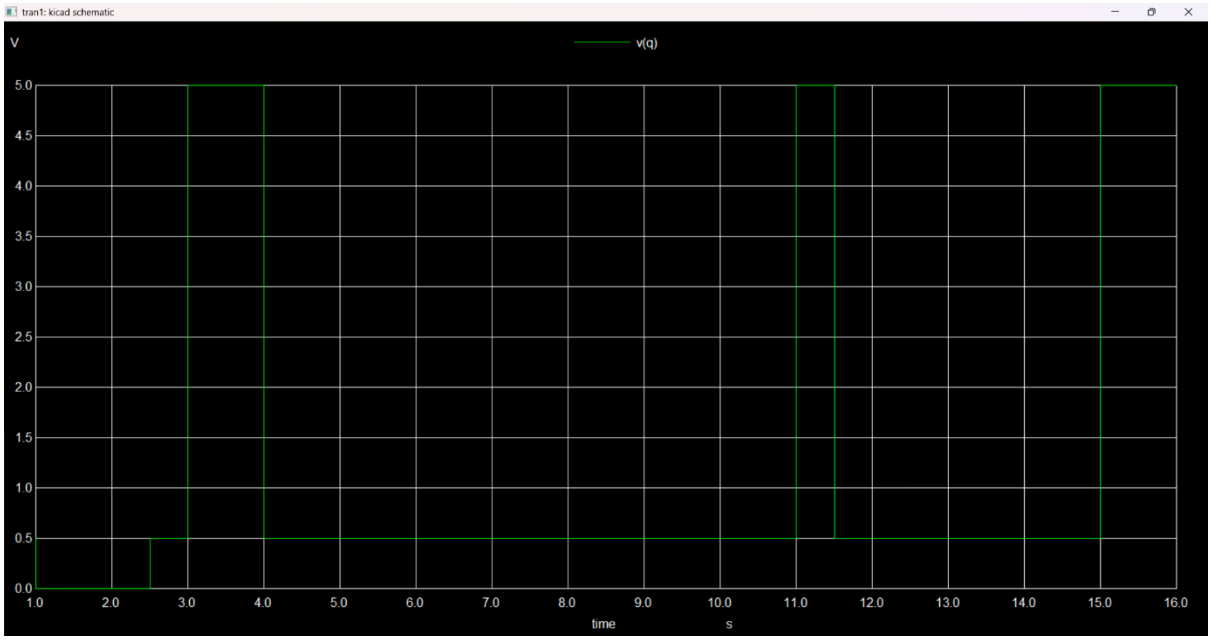
CONTROL INPUTS S & R



CONTROL INPUTS J & K



Output Q



OUTPUT Waveform Explanation

Clk speed – 1 cycle per second

M0 – logic high (1) for 4 sec and logic low (0) for 4sec – total 8 sec for 1 period

M1 – logic high (1) for 8 sec and logic low (0) for 8sec – total 16 sec for 1 period

So the selection lines(M0, M1) goes through all combinations within 16 seconds

M0 = 0 ,M1 = 0 (0 to 4 sec)

D flip flop operation – D input is 0(low logic) for 2 sec and 1(high logic) for 2sec

Q (n+1) output is 0 and 1 respectively for that particular instance

M0 = 1 ,M1 = 0 (4 to 8 sec), Q = 1

T flip flop operation – T input is 0(low logic) for 2 sec and 1(high logic) for 2sec

Q (n+1) output is 0 since clk is not in posedge at T = 1

M0 = 0 ,M1 = 1 (8 to 12 sec), Q = 0

J K flip flop operation – k input is 0(low logic) for 1 sec and 1(high logic) for 1sec

J input is 0(low logic) for 2 sec and 1(high logic) for 2sec

Q (n+1) output is 0 – at j = 0, k = 1

At 11th sec Q(n+1) = 1 as j = 1 k = 1- toggles

M0 = 1 ,M1 = 1 (12 to 16sec), Q = 1

S R flip flop operation – R input is 0(low logic) for 1 sec and 1(high logic) for 1sec

S input is 0(low logic) for 2 sec and 1(high logic) for 2sec

Q (n+1) output is 0 – at r = 1, s = 0 (at 11.5th sec)

Q (n+1) output is 1 – at r = 0, s = 1 (at 15th sec)

Research Paper/Journal/etc. :
Title : Reconfigurable Hardened Latch and Flip-Flop for FPGAs

Authors : Hamzeh Ahangari , Ihsen Alouani, Ozcan Ozturk, Smail Niar

Link : https://ieeexplore.ieee.org/abstract/document/7987558

Source/Reference(s) : Title : *CMOS Digital Integrated Circuits: Analysis and Design*
Author : Sung-Mo Kang, Yusuf Leblebici
Page No : Chapter 7 – Sequential Logic Circuits (Flip-Flops, JK, T, SR, and Universal Structures)