Name of the participant:

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Chennai Institute of Technology

Title of the circuit:

Fine-Grained Clock-Gated 4-Bit Counter for Low-Power Digital Systems

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Theory / Description:

Clock gating is an effective low-power design technique used to reduce dynamic power consumption by disabling the clock to inactive circuit blocks. In conventional synchronous counters, all flip-flops receive the clock irrespective of switching activity, resulting in unnecessary power dissipation.
This circuit implements a **latch-based fine-grained clock gating architecture**, where enable conditions are captured using level-sensitive latches during the low phase of the clock. The latched enable signals are ANDed with the global clock to generate **glitch-free gated clocks** for individual counter bits, allowing only the required flip-flops to toggle.

Reason to reproduce with eSim:

The proposed circuit is well suited for reproduction using **eSim**, as it demonstrates a widely used **industry-standard low-power clock gating technique** in an open-source simulation environment. Migrating this design to eSim enables verification of latch-based glitch-free clock gating without proprietary tools, supports educational learning in low-power VLSI design, and contributes to an open repository of power-efficient digital circuits.

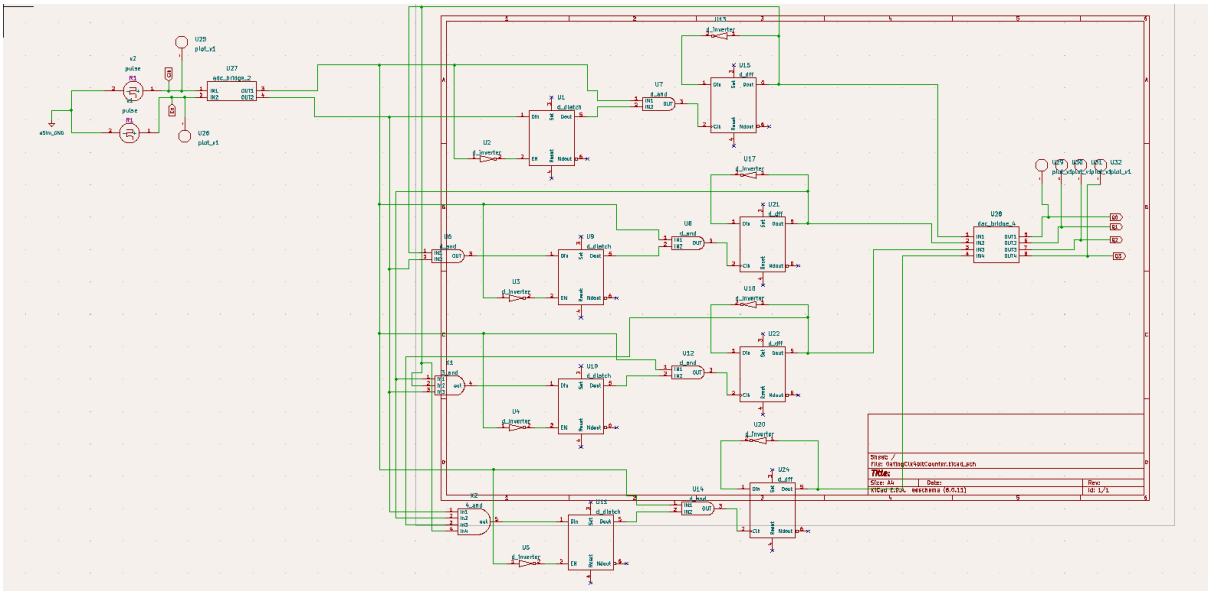
Expected Outcome / Outputs:

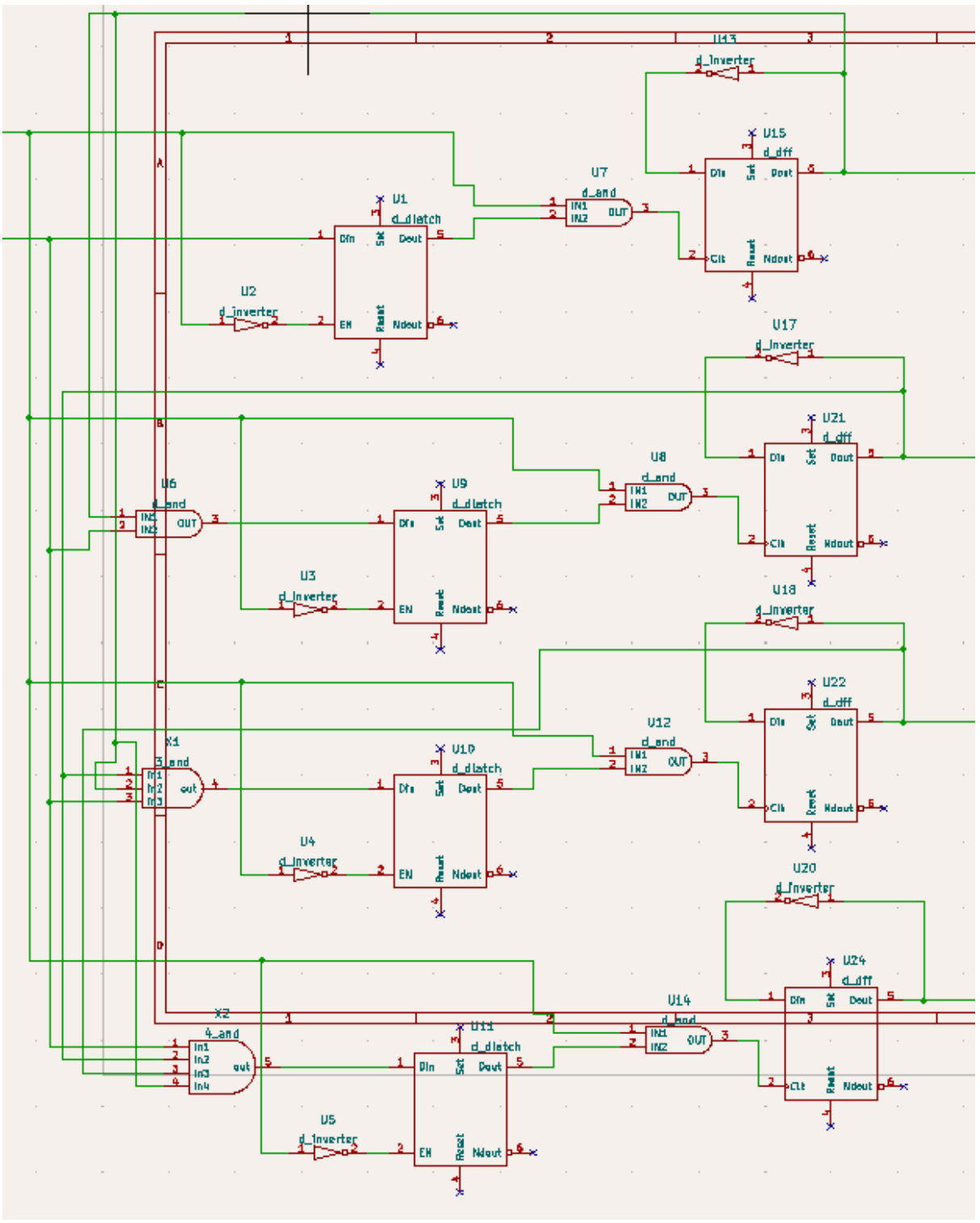
Upon simulation, the counter increments correctly when the enable signal is active, while unused flip-flops remain clock-gated. Individual gated clocks toggle only when required, demonstrating reduced switching activity. The output carry is asserted when all counter bits reach logic high under enable condition, validating correct fine-grained operation.

Circuit Diagram(s):

A complete gate-level schematic consisting of:

- Level-sensitive latches
- AND-based clock gating logic
- D flip-flops
- Inverter for clock phase generation




U13
d_inverter
U15
d_dff
U7
d_and
U1
d_dlatch
U2
d_inverter
U17
d_inverter
U21
d_dff
U8
d_and
U6
d_and
U9
d_dlatch
U3
d_inverter
U18
d_inverter
U22
d_dff
U12
d_and
X1
3_and
U10
d_dlatch
U4
d_inverter
U20
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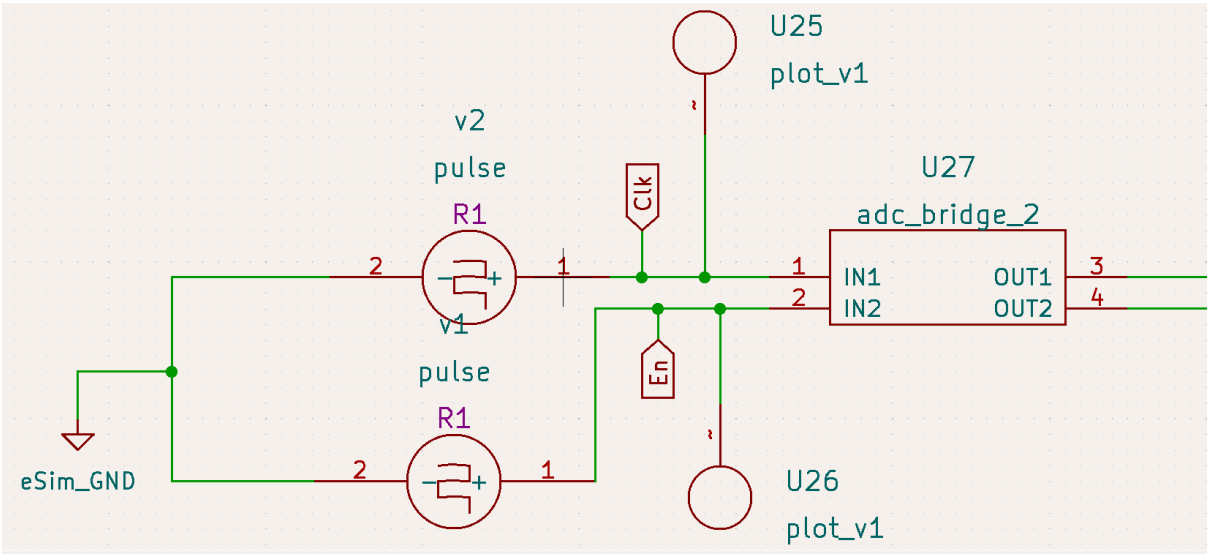
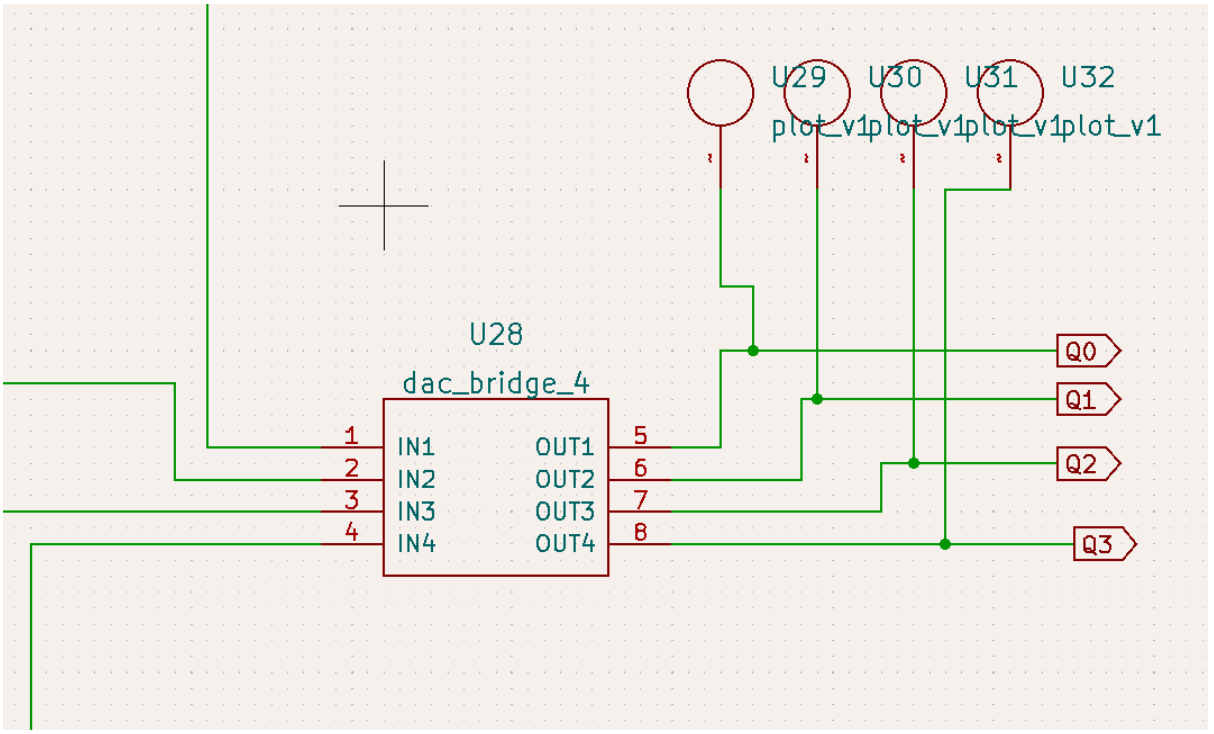
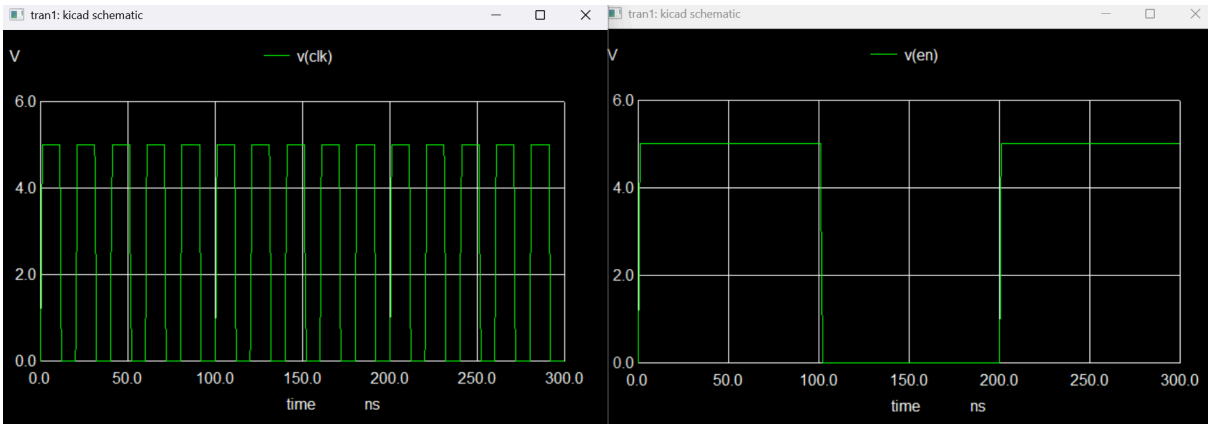
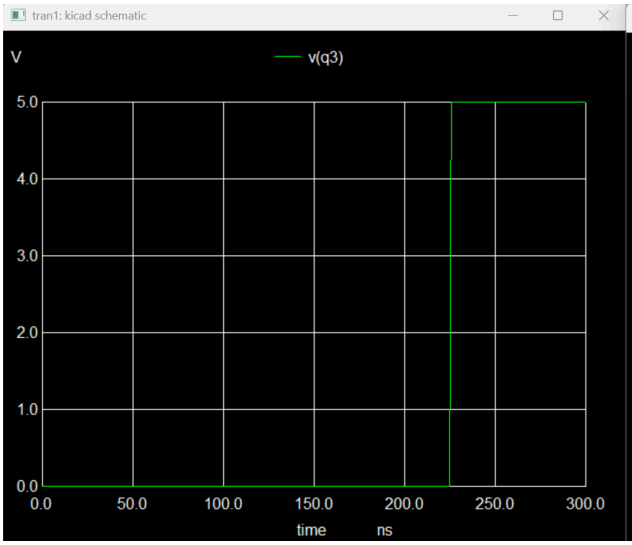
U24
d_dff
U14
d_and
X2
4_and
U11
d_dlatch
U5
d_inverter

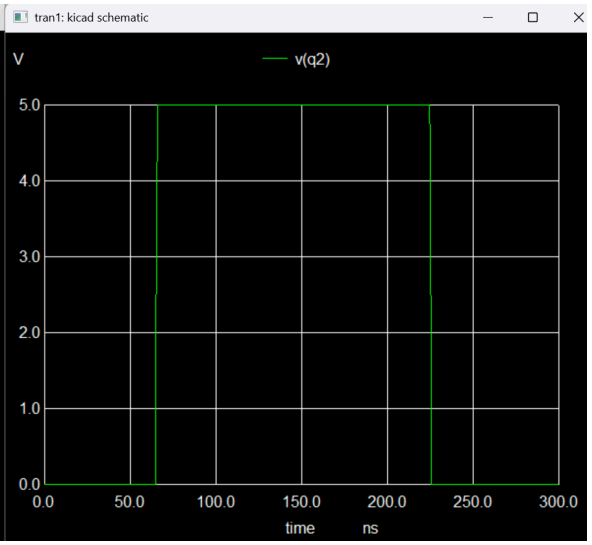


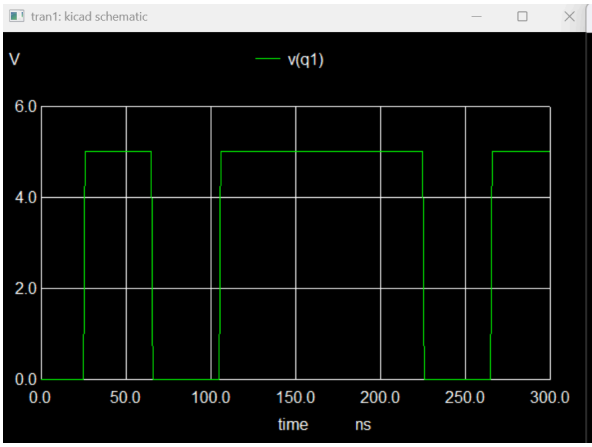


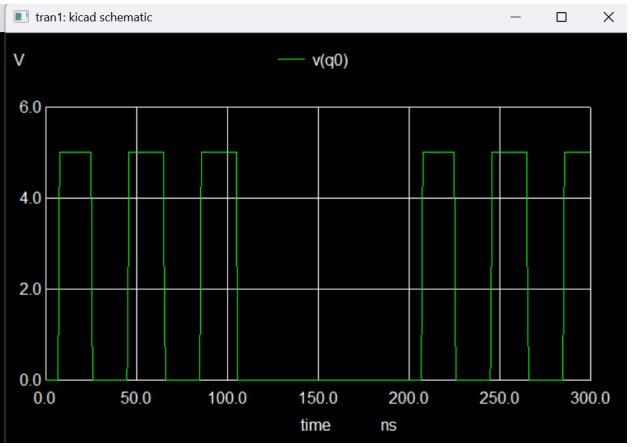
Simulation Output :

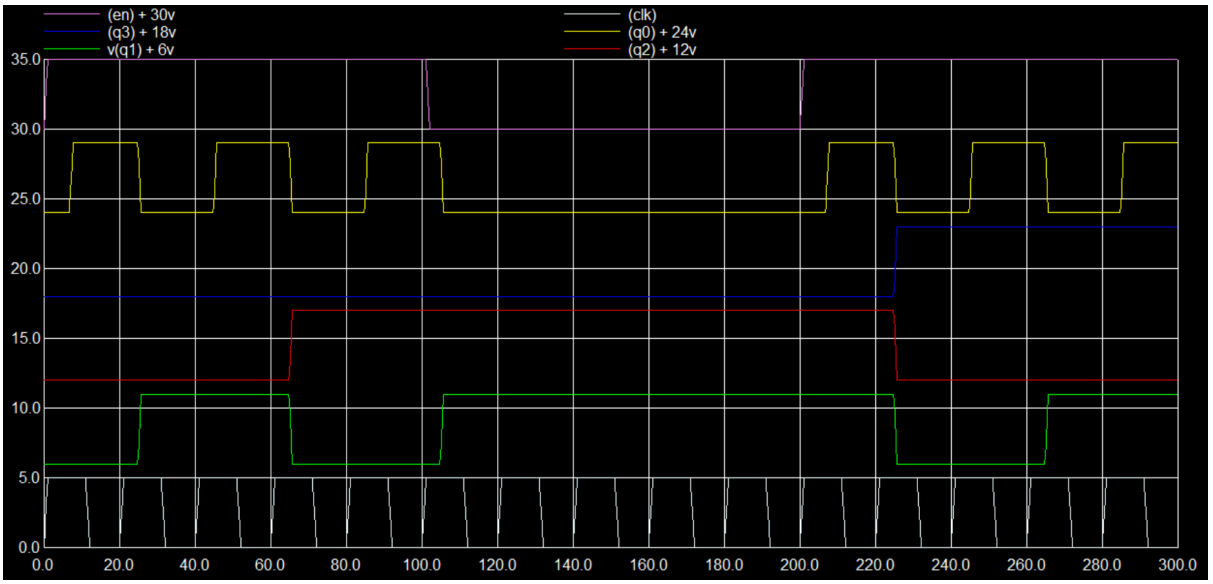



tran1: kicad schematic
V
v(q3)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
50.0
100.0
150.0
200.0
250.0
300.0
time
ns


tran1: kicad schematic
V
v(q2)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
50.0
100.0
150.0
200.0
250.0
300.0
time
ns


tran1: kicad schematic
V
v(q1)
6.0
4.0
2.0
0.0
0.0
50.0
100.0
150.0
200.0
250.0
300.0
time
ns


tran1: kicad schematic
V
v(q0)
6.0
4.0
2.0
0.0
0.0
50.0
100.0
150.0
200.0
250.0
300.0
time
ns


(en) + 30v
(q3) + 18v
v(q1) + 6v
(clk)
(q0) + 24v
(q2) + 12v
35.0
30.0
25.0
20.0
15.0
10.0
5.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
220.0
240.0
260.0
280.0
300.0

Truth table :

En	Clk ↑	Operation
0	↑	Hold (no change)
1	↑	Increment counter

🔹 EN = 1 → Counter increments

Rising CLK @ t(ns)	q3	q2	q1	q0	Decimal
10	0	0	0	1	1
30	0	0	1	0	2
50	0	0	1	1	3
70	0	1	0	0	4
90	0	1	0	1	5

🔸 EN = 0 → HOLD state

Rising CLK @ t(ns)	q3	q2	q1	q0
110	0	1	0	1
130	0	1	0	1
150	0	1	0	1
170	0	1	0	1
190	0	1	0	1

🔹 EN = 1 again → Counter resumes

Rising CLK @ t(ns)	q3	q2	q1	q0	Decimal
210	0	1	1	0	6
230	0	1	1	1	7
250	1	0	0	0	8
270	1	0	0	1	9
290	1	0	1	0	10

Research Paper / Journal / etc.:

Title:
Glitch-Free Clock Gating Techniques for Low-Power Synchronous Circuits

Author:
J. M. Rabaey, A. Chandrakasan, B. Nikolic

Page No.:
Relevant sections on clock gating and low-power sequential logic

Link:
https://ieeexplore.ieee.org/document/1207037

Source / Reference(s):

- J. M. Rabaey et al., *Digital Integrated Circuits: A Design Perspective*, Prentice Hall
- IEEE papers on latch-based clock gating techniques