Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit : Design and CMOS Implementation of Manchester Encoding for Low-Power VLSI Communication Systems

Theory/Description :

Manchester encoding is a digital line coding technique that combines data and clock to enable reliable synchronization. Each data bit is divided into two halves, ensuring a transition at the center of every bit period. A logical '1' is represented by a low-to-high transition, while a logical '0' is represented by a high-to-low transition. The Manchester encoded signal is generated using the relation:

$$\text{Manchester Output} = \text{Data} \oplus \text{Clock}$$

In this design, D flip-flops are used for data synchronization and timing control, while basic logic gates generate the encoded output. The circuit guarantees a mid-bit transition for every input bit, improving clock recovery and transmission reliability.

Reason to reproduce with eSim :

This circuit is suitable for reproduction using eSim due to its open-source nature and support for gate-level and CMOS-based digital design. eSim enables easy simulation and visualization of clock, data, and Manchester-encoded waveforms, allowing clear verification of mid-bit transitions. The platform is ideal for educational and research purposes, as it helps validate theoretical concepts, analyze timing behavior, and compare performance with conventional encoding designs.

Expected Outcome/outputs :

When the circuit is simulated, the output is expected to show a correct Manchester-encoded waveform. For every input data bit, the output will exhibit a guaranteed transition at the midpoint of the bit period. The clock signal will operate at twice the data rate, and the encoded output will follow the relation *Manchester Output = Data ⊕ Clock*.

The correctness of the circuit can be validated by observing the input and output waveforms in the simulator, ensuring proper mid-bit transitions and accurate representation of logical ‘0’ and ‘1’ values.

Circuit Diagrams :

The circuit diagram presents a complete gate-level implementation of a Manchester Encoder for reliable digital communication. It clearly shows how the NRZ data and clock signals are combined to generate a Manchester-encoded output with a guaranteed mid-bit transition.

The circuit consists of the following functional blocks:

- **Clock Input Block:**
  Supplies a square-wave clock operating at twice the data rate, defining bit boundaries and enforcing a transition at the center of each data bit.
- **Data Input Block:**
  Accepts the NRZ data signal, which remains constant for one bit period.
- **Inverter Blocks:**
  Generate complementary versions of the clock and data signals required for Manchester logic.
- **Combinational Logic** (XOR-Equivalent AND–OR Network):
  Basic logic gates are used to implement the relation
  Manchester Output = Data ⊕ Clock,
  ensuring a low-to-high transition for logic ‘1’ and a high-to-low transition for logic ‘0’ at the midpoint of the bit period.
- **Output Node:**
  Produces the final Manchester-encoded waveform with embedded clock information.

All logic connections and signal paths are clearly labeled in the schematic, enabling easy understanding and verification of the Manchester encoding operation through simulation.

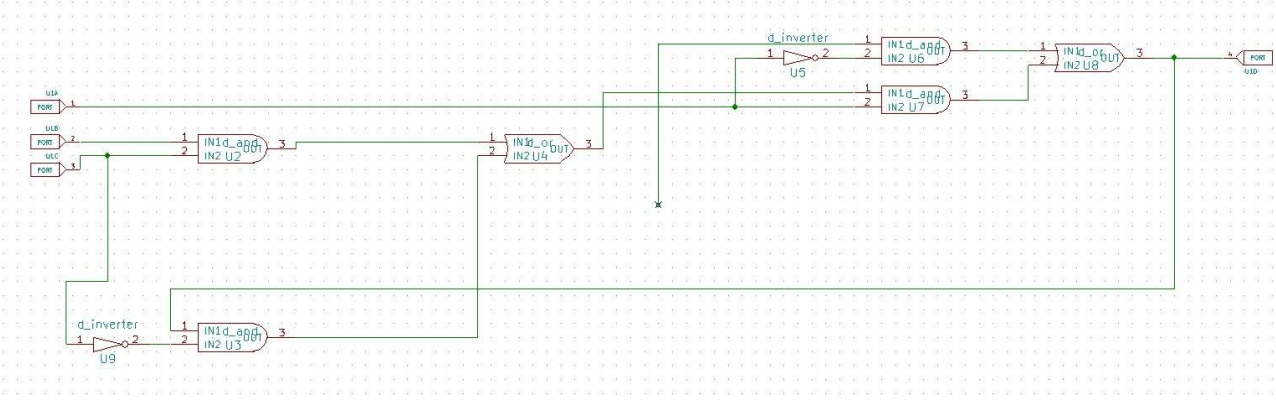

Figure 1 : The schematic implements a Manchester encoder using logic gates. The clock and data inputs are combined to produce an output with a transition at the center of every bit. This ensures correct Manchester encoding and easy verification through simulation.

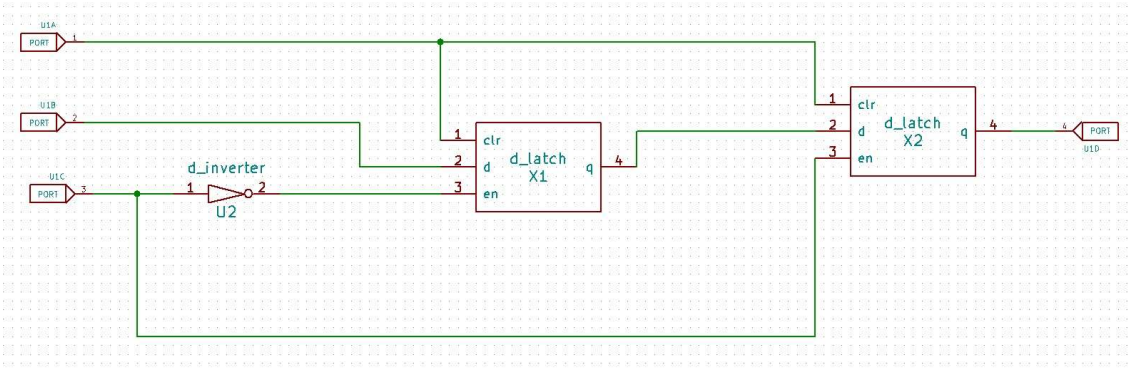

Figure 2 : The D flip-flop stores the input data (D) on the active clock edge and provides a stable output. The clear (CLR) input asynchronously resets the output to zero, ensuring proper initialization of the circuit.

Subcircuit Diagram:

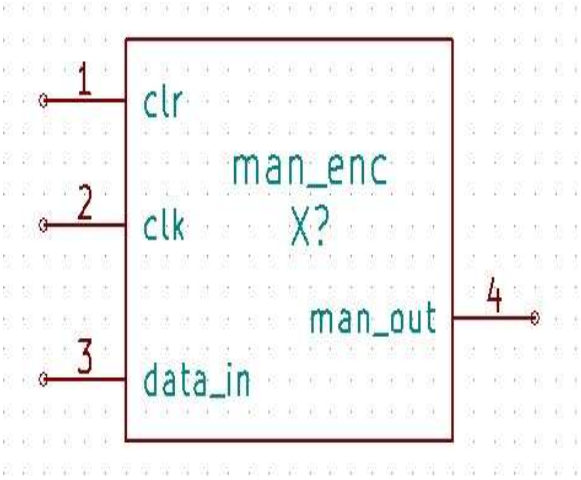

Figure 3 : CMOS-Based Manchester Encoder for NRZ Data Transmission

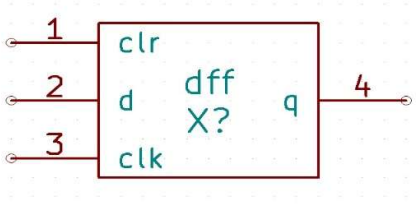

Figure 4 : D Flip-Flop

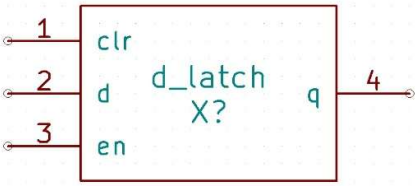

Figure 5 : D latch

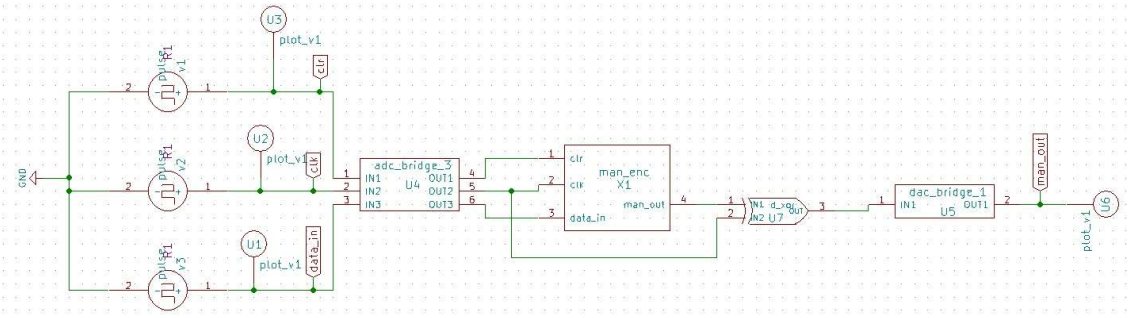

Figure 6 : The test circuit uses a clock source and an NRZ data generator as inputs to the Manchester encoder. An XOR gate is added to combine the clock and data signals, producing the Manchester-encoded output for verification through simulation.

Results:

- Clock Input (clk): Square wave at twice the data rate, 50% duty cycle.
- Data Input (data_in): NRZ signal, stable for one bit period.
- Manchester Output (man_out): XOR of clock and data; each bit shows a mid-bit transition (1 → low-to-high, 0 → high-to-low).
- Waveform & Voltage: Clean rectangular waveforms; logic levels 0 V (0) and Vdd (1).
- Verification: Output transitions align with clock edges; simulation confirms correct Manchester encoding.

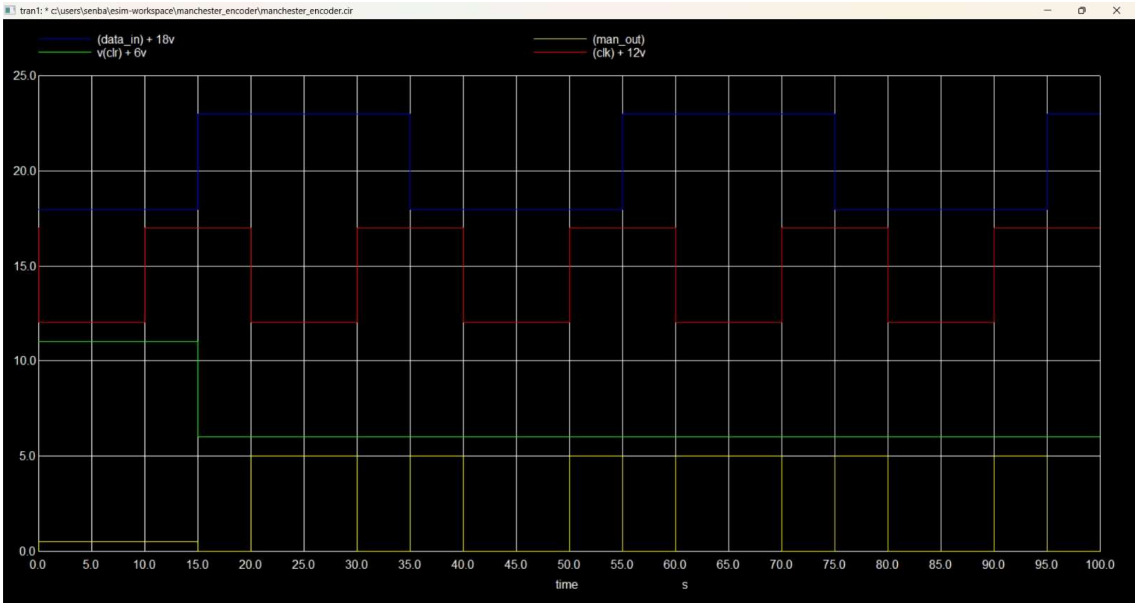

Figure 7 : Simulation Output – Stacked

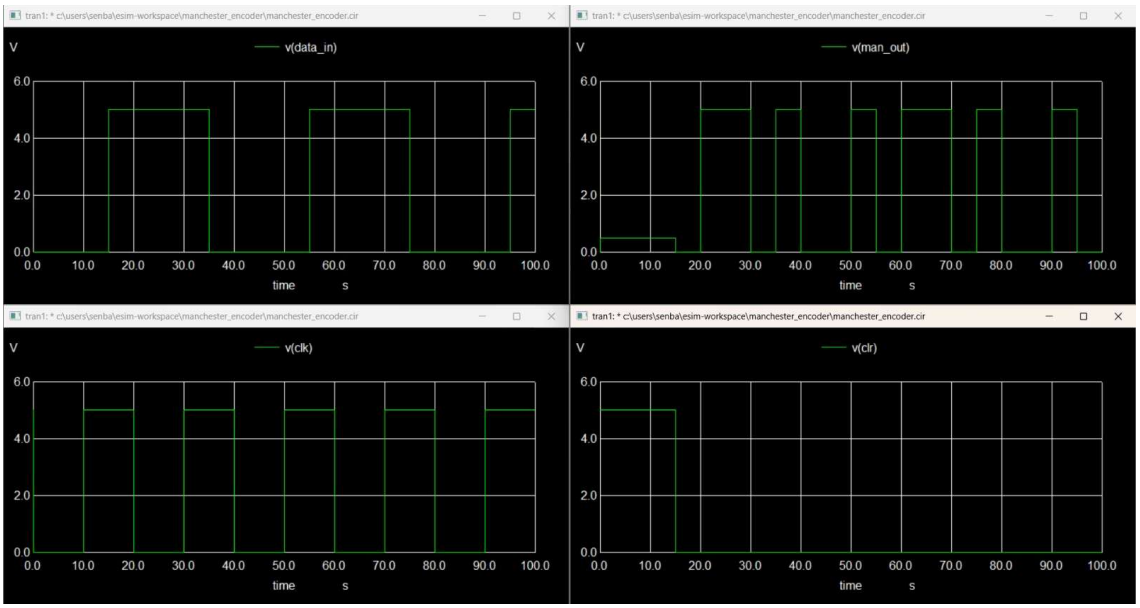

Figure 8 : Separated In and Out Signals

State Table :

Data Bit	First Half of Bit	Second Half of Bit	Mid-Bit Transition
0	High	Low	High → Low
1	Low	High	Low → High

When the clock is XORed with the NRZ data, the output toggles at the midpoint of every bit. A data '1' results in a low-to-high transition, while a data '0' results in a high-to-low transition.

Where to look in graph:

1. **Bit Period:** Defined by v(clk). Each bit lasts from one rising edge to the next (e.g., 20s to 40s).
2. **The Proof**: Look at v(man_out) at exactly 30s, 50s, and 70s.
    - At 30s, notice the signal drops from 5V to 0V.
    - At 50s, notice the signal rises from 0V to 5V.
3. **The Conclusion**: Because every single bit contains a voltage change at the exact midpoint of the clock cycle, it is confirmed as Manchester encoding.

Research Paper/Journal/etc:

IEEE 802.3 Manchester Encoding Reference

Under the IEEE 802.3 Ethernet standard, Manchester encoding is defined based on the direction of the mid-bit transition:

- Logic '0' → High-to-Low transition at the center of the bit period
- Logic '1' → Low-to-High transition at the center of the bit period

The key requirement of the IEEE 802.3 standard is the mandatory mid-bit transition, which enables reliable clock recovery at the receiver.

Note:
The simulation follows the Thomas/GE Manchester convention, which inverts the transition directions compared to IEEE 802.3. Both conventions are valid, as Manchester encoding is defined by the guaranteed mid-bit transition, not the transition polarity.

Title: IEEE Standard for Ethernet
Standard: IEEE 802.3™ – Ethernet
Organization: Institute of Electrical and Electronics Engineers (IEEE)
Link: https://standards.ieee.org/standard/802_3.html